```
   19apr04 13:01:12 User267149 Session D1344.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2004/Apr W2
         (c) 2004 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS 1964-2004/Apr W3
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
  File   8:Ei Compendex(R) 1970-2004/Apr W2
         (c) 2004 Elsevier Eng.  Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci 1990-2004/Apr W2
         (c) 2004 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online 1861-2004/Mar
         (c) 2004 ProQuest Info&Learning
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  File  94:JICST-EPlus 1985-2004/Apr W1
         (c)2004 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Mar
         (c) 2004 The HW Wilson Co.
  File 144:Pascal 1973-2004/Apr W2
         (c) 2004 INIST/CNRS
  File 305:Analytical Abstracts 1980-2004/Apr W2
         (c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2004/Mar
         (c) 2004 DECHEMA
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200425
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/Mar
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

```
Set     Items   Description
S1         55   AU=(GALVAGNI, J? OR GALVAGNI J?)
S2          9   S1 AND ((PRINT??????(3N)CIRCUIT???????) OR (CIRCUIT???????-
                 ?(3N)BOARD???) OR PCB)
S3          7   RD (unique items)
S4         46   S1 NOT S2
S5         35   S4 AND (PASSIV?(3N)COMPONENT? ? OR RESISTOR? ? OR CAPACITO-
                 R? ? OR VARISTOR? ? OR THERMISTOR? ?)
S6          1   S5 AND (INTEGRAT?(1N)PASSIV? OR INTEGRAT?(1N)PASSIV?(1N)DE-
                 VICE? ? OR IPD OR IPDS)
S7         34   S5 NOT S6
S8          0   S7 AND ((VIA OR VIAS OR (VIRTUAL (W) INTERFACE (W)ARCHITEC-
                 TURE) OR HOLE? ? OR GROOVE? ? OR CHANNEL? ? OR EDGE? ? OR TRE-
                 NCH?? OR PATHWAY? ?)(3N)DRILL?)
S9          0   S7 AND (FIBERGLASS? OR FIBER()GLASS?)(3N)COMPOSIT?
```

3/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6250838 INSPEC Abstract Number: B1999-06-2210D-036
Title: Future trend towards integral passives
Author(s): Rector, J.; Dougherty, J.; Brown, V.; **Galvagni**, **J.**; Prymak, J.
Author Affiliation: IBM Corp., Charleston, SC, USA
Conference Title: 17th Capacitor and Resistor Technology Symposium. CARTS '97 p.1-15
Publisher: Components Technol. Inst, Huntsville, AL, USA
Publication Date: 1997 Country of Publication: USA 326 pp.
Material Identity Number: XX-1997-01941
Conference Title: Proceedings of CARTS USA 1997
Conference Sponsor: Components Technol. Inst.; IEEE; Int. Microelectron. & Packaging Soc
Conference Date: 24-27 March 1997 Conference Location: Jupiter, FL, USA
Language: English
Abstract: Integral passive devices are resistors, capacitors, inductors and integrated networks that are an integral part of the interconnect substrate (PWB). Greater miniaturization, product function and performance drive the need for higher component density and improved component performance. Eventually, component density and performance requirements will force manufacturers to integrate the passive components within the PWB. The obstacles which must be overcome to implement integral passives are very significant. Firstly, integral passives profoundly change the design process and much characterization and modeling must be done to allow designers easy transition from use of discretes to integral passives. Since passives will become part of the PWB process, tools and methods must also be developed to reduce the added turnaround time which will probably be required to make design changes in boards using integrated passives. Since a high density interconnection substrate is an inherent primary element and the essential part of the integral passive component manufacturing process, a forward thinking interconnect substrate and passive component industry is essential to reclaiming the electronics manufacturing infrastructure. Electronic design engineers, passive component and interconnection substrate manufacturers together have an opportunity to create this new manufacturing infrastructure. The ultimate objective of this new paradigm is to point the way towards smaller, faster and less expensive electronic products that get to market first and perform reliably for their consumers.
Subfile: B

3/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5704124 INSPEC Abstract Number: B9711-2210D-004
Title: Integrated and integral passive components: a technology roadmap
Author(s): Rector, J., Jr.; Dougherty, J.; Brown, V.; **Galvagni**, **J.**; Prymak, J.
Author Affiliation: IBM Corp., Mt. Pleasant, SC, USA
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.713-23
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595

U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: Integral passive devices are resistors, capacitors, inductors and integrated networks that are an integral part of the interconnection substrate (printed wiring board). Miniaturization, increased product function and performance are driving the need for higher component density and improved component performance. Eventually component density and performance requirements will force hand held product manufacturers to integrate the passive components within the printed wiring board (PWB). This paper is the work of the Passive Component Technology Working Group (P-TWG) of the National Electronics Manufacturing Initiative (NEMI). NEMI is a privately funded initiative created to promote collaborative development by industry, government and academia of the underlying technology and infrastructure required to facilitate manufacture of new high-technology electronic products in North America. The obstacles which must be overcome to implement integral passives are very significant. First of all, integral passives will profoundly change the design process and much characterization and modeling must be done to allow designers to easily transition from use of discretes to integral passives. Since passives will become part of the PWB process, tools and methods must also be developed which reduce the added turnaround time which will probably be required to make design changes in boards using integrated passives. Since a high density interconnection substrate is an inherent primary element and the essential part of the manufacturing process of integral passive components, a vital forward thinking interconnect substrate and passive component industry is essential to reclaiming the electronics manufacturing infrastructure. Electronic design engineers, passive component and interconnection substrate manufacturers together have an opportunity to create this new manufacturing infrastructure. The ultimate objective of this new paradigm is to point the way towards smaller, faster and less expensive electronic products that get to market first and perform reliably for their consumers.
Subfile: B

3/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06182767
E.I. No: EIP02447173107
Title: Controlling capacitor parasitics for high frequency decoupling
Author: Korony, George; Ritter, Andrew; Gonzalez-Titman, Carlos; Hock, Joseph; **Galvagni, John**; Heistand II, Robert
Corporate Source: AVX Corporation, Myrtle Beach, SC 29577, United States
Conference Title: 2001 International Symposium on Microelectronics
Conference Location: Baltimore, MD, United States Conference Date: 20011009-20011011
E.I. Conference No.: 60077
Source: Proceedings of SPIE - The International Society for Optical Engineering v 4587 2001. p 605-609
Publication Year: 2001
CODEN: PSISDG ISSN: 0277-786X
Language: English

Abstract: The need of decoupling power planes at ever-higher frequencies drives the design and production of very low inductance and controlled series resistance capacitors. The loop impedance model, usually applied to the board design, can also help in designing new low inductance high frequency decoupling capacitors. The capacitor structures with current-cancellation and array termination have an approximate three order of magnitude lower inductance than the usual MLCs. The testing of such low inductance capacitors is not a trivial question and needs carefully designed test boards and measuring methods. 8 Refs.

3/3,AB/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015582758
WPI Acc No: 2003-644915/200361
XRAM Acc No: C03-176277
XRPX Acc No: N03-513019
Manufacture of multi-layer electronic devices involves inserting individual passive components vertically into each via, filling via with non-conductive material, and forming electrical connections
Patent Assignee: AVX CORP (AVXA-N)
Inventor: **GALVAGNI J L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030087498	A1	20030508	US 20016777	A	20011108	200361	B

Priority Applications (No Type Date): US 20016777 A 20011108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030087498	A1		18	H01L-021/20	

Abstract (Basic): US 20030087498 A1
Abstract (Basic):
NOVELTY - Multi-layer electronic devices are made by:
(i) inserting individual passive components vertically into each via;
(ii) bonding each passive component to its capture pad;
(iii) filling the via with a non-conductive material; and
(iv) forming electrical connections between each passive component and a portion of second resistive/conductive patterns on an outer surface of a unitary device body.
DETAILED DESCRIPTION - Manufacture of multi-layer electronic devices includes:
(a) providing a first device layer with a first series of resistive/conductive patterns;
(b) providing a second device layer with vias (40, 42) drilled through the second device layer;
(c) bonding the first and second device layers together to form a unitary body, where each via corresponds to a respective capture pad in the first series of resistive/conductive patterns;
(d) providing a second series of resistive/conductive patterns on an outer layer of the unitary body;
(e) providing terminations on the unitary body for electrical connection to other electronic devices;
(f) inserting individual passive components (14) vertically into each via;
(g) bonding each passive component to its respective capture pad;

(h) filling the via with a non-conductive material; and

(i) forming electrical connections between each passive component and a portion of the second resistive/conductive patterns on an outer surface of the unitary device body.

USE - For manufacturing multi-layer electronic devices (claimed), i.e. a **printed circuit board** (**PCB**) or an integrated passive device (IPD).

ADVANTAGE - The method reduces the space demands placed upon the surface of the **PCB**, enhances the flexibility of circuitry design, and allows for a greater variety of passive components and integral passive devices to be utilized within the **PCB** itself.

It also provides for greater flexibility in the design and manufacture of the IPDs by allowing for the vertical electrical connection of various passive components through the placement of intervening passive components into the via. It allows for the vertical orientation of various types of passive components within a layer of the **PCB** or the IPD.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section view of a **printed circuit board**.

Passive components (14)

Vias (40, 42)

pp; 18 DwgNo 4/13

3/3,AB/5 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012289887

WPI Acc No: 1999-095993/199908

XRPX Acc No: N99-069763

Surface mount multi-layer ceramic capacitor for **printed circuit board** - has interleaved electrodes plates with interdigitated lead structures providing multiple, adjacent current injection points onto associated main electrode portion

Patent Assignee: AVX CORP (AVXA-N)

Inventor: DUPRE' D A; **GALVAGNI J L**; RITTER A P; DUPRE D A

Number of Countries: 083 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9900807	A1	19990107	WO 98US9873	A	19980514	199908	B
US 5880925	A	19990309	US 97884597	A	19970627	199917	
AU 9873871	A	19990119	AU 9873871	A	19980514	199922	
EP 995207	A1	20000426	EP 98921208	A	19980514	200025	
			WO 98US9873	A	19980514		
CN 1261457	A	20000726	CN 98806558	A	19980514	200057	
US 6243253	B1	20010605	US 97884597	A	19970627	200133	
			US 99264124	A	19990308		
KR 2001020511	A	20010315	KR 99712280	A	19991224	200159	
JP 2002508114	W	20020312	WO 98US9873	A	19980514	200220	
			JP 99505532	A	19980514		

Priority Applications (No Type Date): US 97884597 A 19970627; US 99264124 A 19990308

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9900807	A1	E	34	H01G-004/005	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM

TR TT UA UG UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

US 5880925	A		H01G-004/005	
AU 9873871	A			Based on patent WO 9900807
EP 995207	A1 E		H01G-004/005	Based on patent WO 9900807
Designated States (Regional): BE CH DE DK ES FI FR GB IE IT LI NL SE				
CN 1261457	A		H01G-004/005	
US 6243253	B1		H01G-004/228	Cont of application US 97884597 Cont of patent US 5880925
KR 2001020511	A		H01G-004/005	
JP 2002508114	W	27	H01G-004/12	Based on patent WO 9900807

Abstract (Basic): WO 9900807 A

The capacitor comprises a low-aspect capacitor body including first and second electrode plates (58,60) interleaved in opposed and spaced apart relation. Layers of dielectric material to provide a predetermined dielectric constant separate the electrode plates. Each of the first and second electrode plates includes a main electrode portion (64,68) and spaced apart lead structures (66,70) extending from it, respective lead structures of the first electrode plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement. Corresponding lead structures of respective first electrode plates are electrically connected together and corresponding lead structures of respective second electrodes plates are electrically connected together to define electrical terminals of a first polarity and electrical terminals of a second polarity, respectively. Preferably, the electrical terminals are formed by a thick-film terminal material.

ADVANTAGE - Low inductance. Offset nature of lead structure on opposite lateral sides of each electrode plate also reduces mutual inductance levels.

Dwg.6/11

3/3,AB/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010188205
WPI Acc No: 1995-089458/199512
XRPX Acc No: N95-070730

Trapezoid chip ceramic capacitor - is formed on isosceles trapezoid in longitudinal section, e.g. termination is effected by placing larger base on support surface and stacking number of trapezoidal capacitors in side-to-side relationship

Patent Assignee: AVX CORP (AVXA-N)
Inventor: **GALVAGNI J**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5388024	A	19950207	US 93100375	A	19930802	199512	B

Priority Applications (No Type Date): US 93100375 A 19930802
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5388024	A		6	H01G-001/14	

Abstract (Basic): US 5388024 A

The capacitor assembly includes a number of discrete radially

separable interconnected ceramic capacitors arranged in a stack. Each of the capacitors has mutually spaced first and second opposite polarity terminals. The latter in one of capacitors in the stack are disposed in abutting relation to the terminals of adjacent capacitors.

Continuous first and surface conductive readily fractured termination films couple respective first and second termination of the capacitors in the stack. Hence individual capacitors or capacitors gp of mechanically and electrically connected capacitors as sub-unit may be separated from the stack.

USE/ADVANTAGE - As multiple capacitors stack for soldering on personal computer board. Minimised possibility of soldering connection will short **circuit** other elements on **board** with improved use of generator board, and easier termination.

Dwg.1-3/7

3/3,AB/7 (Item 1 from file: 371)
000884090
Title: Condensateur du type solide pour montage en surface, a faible encombrement, et son procede de fabrication.
Patent Applicant/Assignee: AVX CORP
Applicant Address: AVX CORPORATION- Deposant - 750 LEXINGTON AVENUE, NEW YORK, NEW YORK 10022 ETATS UNIS D'AMERIQUE (US)
Inventor(s): **GALVAGNI JOHN** - P.O. BOX 560, MYRTLE BEACH, SOUTH CAROLINA 29578-0560 ETATS UNIS D'AMERIQUE (US
Legal Representative: BEAU DE LOMENIE
Document Type: Patent / Brevet
Patent and Priority Information (Country, Number, Date):
Patent: FR 2694124 - 19940128
Application: FR 936048 - 19930519
Priority Application: US 92917848 - 19920723

Abstract:
L'invention concerne un condensateur au tantale du type a monter en surface ainsi qu'un procede permettant de le fabriquer. Selon ce procede, on remplit completement ou partiellement un conteneur de tantale tubulaire (20) a l'aide de poudre de tantale (21), on effectue un frittage afin de lier la poudre a elle-meme et au conteneur, puis on effectue un traitement classique afin de former un revetement dielectrique et un revetement de contre-electrode. On fixe une terminaison d'anode (26) a une surface externe du conteneur et on fixe une terminaison de cathode (25) a une partie de la contre-electrode exposee via une ouverture menagee dans le conteneur. Le condensateur resultant se distingue par une capacite elevee par unite de volume, un petit encombrement en surface, une grande resistance aux chocs et une faible resistance serie equivalente.

Legal Status (Type, Action Date, BOPI No, Description):

Publication	19940128	9404	Date published
Search Report	19940211	9406	Date Search Report published
Grant	19941104	9444	Date granted

6/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015888072
WPI Acc No: 2004-045907/200405
XRAM Acc No: C04-018757
XRPX Acc No: N04-037482
Multilayer electronic component e.g. multilayer interdigitated **capacitor**, includes plated termination to which tabs of central electrodes interleaved between insulating substrates, are connected
Patent Assignee: AVX CORP (AVXA-N); DATTAGURU S (DATT-I); GALVAGNI J L (GALV-I); HEISTAND R (HEIS-I); MACNEAL J (MACN-I); RITTER A P (RITT-I)
Inventor: DATTAGURU S; **GALVAGNI J L**; HEISTAND R; MACNEAL J; RITTER A; HEISTAND R H; RITTER A P
Number of Countries: 005 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2389708	A	20031217	GB 20038656	A	20030415	200405 B
DE 10316983	A1	20031224	DE 1016983	A	20030411	200406
US 20030231457	A1	20031218	US 2002372673	P	20020415	200410
			US 2003409023	A	20030408	
JP 2004040084	A	20040205	JP 2003109640	A	20030414	200411
JP 2004040085	A	20040205	JP 2003109641	A	20030414	200411
US 20040022009	A1	20040205	US 2002372673	P	20020415	200411
			US 2002435218	P	20021219	
			US 2003409036	A	20030408	
CN 1459808	A	20031203	CN 2003145440	A	20030415	200413

Priority Applications (No Type Date): US 2003409036 A 20030408; US 2002372673 P 20020415; US 2002435218 P 20021219; US 2003409023 A 20030408
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2389708	A		55	H01G-004/232	
DE 10316983	A1			H01G-004/01	
US 20030231457	A1			H01G-004/228	Provisional application US 2002372673
JP 2004040084	A		63	H01G-004/252	
JP 2004040085	A		75	H01G-004/30	
US 20040022009	A1			H01G-004/228	Provisional application US 2002372673
					Provisional application US 2002435218
CN 1459808	A			H01G-004/005	

Abstract (Basic): GB 2389708 A
Abstract (Basic):
NOVELTY - The electrodes (110,112) interleaved between the insulating substrates, include tabs (114,116) of different length and width. The tabs of central electrodes are connected to a plated termination (130).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) multilayer electronic component manufacturing method; and
(2) plating layer formation directing method.
USE - E.g. multilayer interdigitated **capacitor** and **integrated passive component**.
ADVANTAGE - The need for thick film termination stripes is eliminated and the **capacitor** is provided with plated termination.

DESCRIPTION OF DRAWING(S) - The figure shows the side cross

sectional view of **capacitor** and exploded plane view of electrodes.

capacitor (100)
electrodes (110,112)
tabs (114,116)
plated termination (130)
solder ball (140)
pp; 55 DwgNo 5, 6/21

```
 19apr04 13:27:38 User267149 Session D1345.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2004/Apr W2
         (c) 2004 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS 1964-2004/Apr W3
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  File   8:Ei Compendex(R) 1970-2004/Apr W2
         (c) 2004 Elsevier Eng.  Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci 1990-2004/Apr W2
         (c) 2004 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online 1861-2004/Mar
         (c) 2004 ProQuest Info&Learning
  File  65:Inside Conferences 1993-2004/Apr W2
         (c) 2004 BLDSC all rts. reserv.
  File  94:JICST-EPlus 1985-2004/Apr W1
         (c)2004 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Mar
         (c) 2004 The HW Wilson Co.
  File 144:Pascal 1973-2004/Apr W2
         (c) 2004 INIST/CNRS
  File 305:Analytical Abstracts 1980-2004/Apr W2
         (c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2004/Mar
         (c) 2004 DECHEMA
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200425
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/Mar
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
```

```
Set     Items   Description
S1     323816   (PRINT??????(3N)CIRCUIT???????) OR (CIRCUIT????????(3N)BOA-
             RD???) OR PCB
S2     721168   PASSIV?(3N)COMPONENT? ? OR RESISTOR? ? OR CAPACITOR? ? OR -
             VARISTOR? ? OR THERMISTOR? ?
S3       5671   INTEGRAT?(1N)PASSIV? OR INTEGRAT?(1N)PASSIV?(1N)DEVICE? ? -
             OR IPD OR IPDS
S4     725548   S2:S3
S5    7589719   LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()-
             LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER?????
              OR MULTIPLE()LAYER? ?
S6      76369   (RESIST? OR CONDUCT?)(3N)PATTERN? ?
S7      60016   (VIA OR VIAS OR (VIRTUAL (W) INTERFACE (W)ARCHITECTURE) OR
             HOLE? ? OR GROOVE? ? OR CHANNEL? ? OR EDGE? ? OR TRENCH?? OR -
             PATHWAY? ?)(3N)DRILL?
S8     566622   (EPOX??? OR RESIN? ? OR THERMOPLASTIC??? OR THERMO()PLASTI-
             C???  OR THERMOSET? OR ELASTOMER?? OR RUBBER? ? OR ADHESIVE??-
             )(3N)(LAYER??? OR FILM??? OR COAT???)
S9     243580   (RESINOUS? OR POLYMER? OR SYNTHETIC?)(2N)(MATERIAL? OR SUB-
             STANCE? OR MOLD? OR CAST?)
S10    809685   PHENOLIC? OR ALKYD? OR  POLYESTER? OR EPOXIDE OR SILICONE
S11   4772586   (POLYMER???? OR HOMOPOLYMER????? OR COPOLYMER????? OR TERP-
             OLYMER? OR RESIN? OR GUM?)
S12   8104468   ADHESIVE? ? OR ADHERE??? OR ATTACH??????? OR SECUR??????? -
             OR CONNECT???????? OR STICK???????? OR SEAL????????
S13   2236393   PLASTIC? OR THERMOPLASTIC? OR THERMOSET? OR (RESINOUS? OR -
             POLYMER? OR SYNTHETIC?)(3N)(MATERIAL? OR SUBSTANCE? OR MOLD? -
             OR CAST?)
S14     18897   MC=(X12-E02B OR T03-A01A3)
S15     16724   FIBERGLASS? OR FIBER()GLASS?
S16      2029   (FIBERGLASS? OR FIBER()GLASS?)(3N)COMPOSIT?
S17     16724   S15:S16
S18      3817   UNITAR?(3N)BODY OR BOND?(3N)UNION? ?
S19      4193   (ELECTRIC? OR OPPOSING OR OPPOSITE? OR CONTRAST?)(3N)TERMI-
             NAT?
S20     30226   NON()CONDUCT?
S21    260303   ELECTRIC?(3N)CONNECT?
S22    390909   SOLDER(W)BOND? OR SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
S23     30665   (SOLDER?)(W)(BALL? ? OR BUMP? ? OR POST? ? OR SPHERE?) OR -
             BGA OR BALLGRID? ? OR BALL(W)GRID? ? OR POLYMER(W)BALL? ?
S24     12356   (SOLDER(W)BOND? OR SOLDER OR SOLDERING OR SOLDERED OR BRAZ-
             ?)(3N)REFLOW?
S25    400515   S22:S24
Set     Items   Description
S25    400515   S22:S24
S26     15065   S1 AND S4
S27      5728   S26 AND S5
S28       412   S27 AND S6
S29         4   S28 AND S7
S30         4   RD (unique items)
S31       408   S28 NOT S29
S32       261   S31 AND (S8 OR S9 OR S10 OR S11 OR S12 OR S13 OR S14)
S33         0   S32 AND S17
S34         0   S32 AND S18
S35         1   S32 AND S19
S36       260   S32 NOT S35
```

S37	1	S36 AND S20
S38	259	S36 NOT S37
S39	0	S38 AND S20
S40	43	S38 AND S21
S41	7	S40 AND S25
S42	7	RD (unique items)
S43	36	S40 NOT S41
S44	36	RD (unique items)
S45	36	S44 AND S2
S46	0	S45 AND S3
S47	0	S45 AND S15
S48	0	S45 AND S16
S49	0	S45 AND S24
S50	36	S45
S51	133	S25 AND S17
S52	0	S51 AND S19
S53	0	S51 AND S18
S54	2	S51 AND S7
S55	2	RD (unique items)
S56	131	S51 NOT S54
S57	0	S56 AND S7
S58	54	S56 AND S5
S59	46	S58 AND (S8 OR S9 OR S10 OR S11 OR S12 OR S13 OR S14)
S60	46	RD (unique items)
S61	46	S60 NOT S29,S35,S37,S40,S55
S62	24	S61 AND S1

30/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03028736 INSPEC Abstract Number: B88001025
Title: Improved performance of hybrid microwave thin **film** circuits (HMICs) using through-hole connections (THCs)
Author(s): Bassani, C.; Ferraris, G.P.; Villa, C.; Ziboni, M.
Author Affiliation: GTE Telecomunicazioni, Milano, Italy
Conference Title: Sixth European Microelectronics Conference Proceedings. ISHM Europe '87 p.240-50
Publisher: Int. Soc. Hybrid Microelectron. Eur, London, UK
Publication Date: 1987 Country of Publication: UK 494 pp.
Conference Date: 3-5 June 1987 Conference Location: Bournemouth, UK
Language: English
Abstract: Low inductance integrated through-connections between the front surface and the corresponding back surface pattern or ground plane have been requested for a long time by designers and manufacturers of HMICs. Existing technology and manufacture economy impose severe constraints on conductive via process development, principal fixed constraints being: utilization of the existing **resistor**/conductor technology-laser **hole drilling** on patterned and stabilized circuits-no further step in vacuum deposition equipment, as the authors want to purchase metallized substrates on the present market, if necessary, and have them in stock for subsequent photolithography. These constraints have left few possibilities in the choice of the process, because it is implicit that the authors had to follow the chemical method of metal deposition, as in **printed circuit board** technology. The major problem in adopting this process is to obtain good metallization adhesion to ceramic substrate and on this topic the efforts were concentrated with good results. The conductive via processing begins when the thin **film** patterning is finished and the tantalum **resistors** are stabilized. **Conductor pattern** is used to locate the position of laser drills.
Subfile: B

30/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015582758
WPI Acc No: 2003-644915/200361
XRAM Acc No: C03-176277
XRPX Acc No: N03-513019
Manufacture of **multi-layer** electronic devices involves inserting individual **passive components** vertically into each via, filling via with non-conductive material, and forming electrical connections
Patent Assignee: AVX CORP (AVXA-N)
Inventor: GALVAGNI J L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030087498	A1	20030508	US 20016777	A	20011108	200361	B

Priority Applications (No Type Date): US 20016777 A 20011108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030087498	A1		18	H01L-021/20	

Abstract (Basic): US 20030087498 A1
Abstract (Basic):
NOVELTY - **Multi-layer** electronic devices are made by:
(i) inserting individual **passive components** vertically into each via;
(ii) bonding each **passive component** to its capture pad;

(iii) filling the via with a non-conductive material; and
(iv) forming electrical connections between each **passive component** and a portion of second **resistive/conductive patterns** on an outer surface of a unitary device body.
DETAILED DESCRIPTION - Manufacture of **multi-layer** electronic devices includes:
(a) providing a first device **layer** with a first series of **resistive/conductive patterns**;
(b) providing a second device **layer** with **vias** (40, 42) **drilled** through the second device **layer**;
(c) bonding the first and second device **layers** together to form a unitary body, where each via corresponds to a respective capture pad in the first series of **resistive/conductive patterns**;
(d) providing a second series of **resistive/conductive patterns** on an outer **layer** of the unitary body;
(e) providing terminations on the unitary body for electrical connection to other electronic devices;
(f) inserting individual **passive components** (14) vertically into each via;
(g) bonding each **passive component** to its respective capture pad;
(h) filling the via with a non-conductive material; and
(i) forming electrical connections between each **passive component** and a portion of the second **resistive/conductive patterns** on an outer surface of the unitary device body.
USE - For manufacturing **multi-layer** electronic devices (claimed), i.e. a **printed circuit board** (**PCB**) or an **integrated passive device** (**IPD**).
ADVANTAGE - The method reduces the space demands placed upon the surface of the **PCB**, enhances the flexibility of circuitry design, and allows for a greater variety of **passive components** and integral **passive** devices to be utilized within the **PCB** itself.
It also provides for greater flexibility in the design and manufacture of the **IPDs** by allowing for the vertical electrical connection of various **passive components** through the placement of intervening **passive components** into the via. It allows for the vertical orientation of various types of **passive components** within a **layer** of the **PCB** or the **IPD**.
DESCRIPTION OF DRAWING(S) - The figure is a cross-section view of a **printed circuit board**.
Passive components (14)
Vias (40, 42)
pp; 18 DwgNo 4/13

30/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04284123
MANUFACTURE OF HYBRID INTEGRATED CIRCUIT DEVICE

PUB. NO.: 05-275823 [JP 5275823 A]
PUBLISHED: October 22, 1993 (19931022)
INVENTOR(s): KAGAWA TOSHIYUKI
APPLICANT(s): TAIYO YUDEN CO LTD [359306] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-096000 [JP 9296000]
FILED: March 24, 1992 (19920324)
JOURNAL: Section: E, Section No. 1498, Vol. 18, No. 53, Pg. 59, January 27, 1994 (19940127)

ABSTRACT

PURPOSE: To accurately regulate **resistors** individually by preventing a conductive **film** from being formed over a through-**hole drilled** on an insulating **circuit board** when **resistors** formed on the **circuit board** are subjected to trimming, thereby hindering the **resistors** from being connected in parallel or connected in a loop through another interconnection **pattern** and **resistors**.

CONSTITUTION: An interconnection pattern and a land electrode are formed on an insulating **circuit board** 1. At this time, a conductive **film** is not formed over the inner peripheral surface of a through-hole 2. Resistive paste is printed and applied between a pair of through-hole land electrodes 3(sub 1) and 3(sub 3) and a pair of through-hole land electrodes 3(sub 2) and 3(sub 4) and calcined, thereby producing **resistors** 4 and 4'. In the laser trimming of the **resistors**, because a conductive **film** is not formed over the through-hole 2, **resistors** that are connected in parallel or connected in a loop through another interconnection **pattern** and **resistors** are never produced. Hence, each **resistor** can be trimmed to an accurate desired resistance value.

30/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03285092
CIRCUIT BOARD

PUB. NO.: 02-260592 [JP 2260592 A]
PUBLISHED: October 23, 1990 (19901023)
INVENTOR(s): OYAMA SADAKIMI
SEKINE NORIAKI
APPLICANT(s): MITSUMI ELECTRIC CO LTD [000622] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-081148 [JP 8981148]
FILED: March 31, 1989 (19890331)
JOURNAL: Section: E, Section No. 1020, Vol. 15, No. 4, Pg. 46, January 08, 1991 (19910108)

ABSTRACT

PURPOSE: To reduce an area occupied by **resistors** and realize a thin and high density printed board by a method wherein the **resistors** are provided in through- **holes drilled** in the board.

CONSTITUTION: Copper wiring patterns 5 are formed on both the sides of a board 1 by printing or plating. Solder resist material 13 is applied to the surfaces of the wiring patterns 5 except the parts for attaching components. Gold plating is applied to the predetermined positions of the wiring patterns 5 to form gold electrodes 2. A bare chip IC 6 is bonded to the wiring pattern with gold wires 7 and a resin **coating** 8 is applied by potting. Further, a chip **capacitor** 9, a chip coil 10, etc., are soldered to the wiring **patterns** 5. By providing **resistors** 4 in the through-holes 12 of the board 1, the resistance element can be eliminated from the surfaces of the **circuit board** 1. With this constitution, an area occupied by the **resistors** can be reduced and a high density **circuit boards** can be realized.

35/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015851576
WPI Acc No: 2004-009403/200401
XRAM Acc No: C04-002478
XRPX Acc No: N04-006681
Printed circuit board comprises **resinous**, electrically insulating substrate, circuit **pattern**, spaced **resistor** terminations, thin **film resistor**, and over-**coating layer** formed of one-part ink
Patent Assignee: SAMSUNG ELECTRO MECHANICS CO LTD (SMSU)
Inventor: KANG J G; LEE S G; PARK K Y; KANG J; LEE S; PARK K
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030150101	A1	20030814	US 200297406	A	20020315	200401	B
CN 1423517	A	20030611	CN 2002108800	A	20020402	200401	
KR 2003046552	A	20030618	KR 200176218	A	20011204	200401	

Priority Applications (No Type Date): KR 200176218 A 20011204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030150101	A1		15	H01C-007/00	
CN 1423517	A			H05K-001/16	
KR 2003046552	A			H05K-001/16	

Abstract (Basic): US 20030150101 A1
Abstract (Basic):
NOVELTY - A **printed circuit board** comprises **resinous**, electrically insulating substrate, circuit **pattern** and spaced **resistor** terminations. Each **resistor** termination comprises a metal pad covered with conductive protective **layer**. A thin **film resistor** is formed between the **resistor** terminations. An over-**coating layer** formed of one-part ink covers the **resistor** and the **resistor** terminations.

DETAILED DESCRIPTION - A **printed circuit board** comprises **resinous**, electrically insulating substrate, circuit **pattern** and spaced **resistor** terminations, in sequence. Each **resistor** termination comprises a metal pad covered with conductive protective **layer**. A thin **film resistor** is formed between the **resistor terminations** with **electrical connection**. An over-**coating layer** formed of one-part ink covers the **resistor** and the **resistor** terminations.

An INDEPENDENT CLAIM is also included for manufacturing a **printed circuit board** (**PCB**) comprising:

(i) building a pair of spaced **resistor** metal pads along with circuit pattern on **resinous** insulating substrate;

(ii) depositing a blanket of a solder mask **layer** over the resulting substrate structure;

(iii) selectively removing the solder mask **layer** to form a solder mask opening though which the **resistor** metal pads and region is exposed;

(iv) forming a conductive protective **layer** on each of the **resistor** metal pads to give **resistor** terminations;

(v) forming a thick **film resistor** between the **resistor terminations** with an **electrical**

connection of the **resistor** to the terminations; and

(vi) covering the **resistor** and the **resistor** terminations with an overcoating **layer** of one-part ink.

USE - **Printed circuit board.**

ADVANTAGE - The **printed circuit board** is embedded with a **resistor** having a resistance that is uniform without being affected by the external environment.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of a **resistor** structure trimmed by a laser.

pp; 15 DwgNo 3a/4

37/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012880158
WPI Acc No: 2000-051991/200004
XRAM Acc No: C00-013320
XRPX Acc No: N00-040541
Manufacturing **connectors** used for mounting electric parts such as integrated circuits
Patent Assignee: POLYPLASTICS CO INC (POPL); SANKYOUKASEI CO LTD (SANB)
Inventor: NISHIKAWA Y; YUMOTO T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5979048	A	19991109	US 95464661	A	19950621	200004 B
			US 97813893	A	19970307	

Priority Applications (No Type Date): US 97813893 A 19970307; US 95464661 A 19950621
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5979048	A		10	H01R-043/00	CIP of application US 95464661

Abstract (Basic): US 5979048 A
Abstract (Basic):
NOVELTY - The method is carried out by molding a resin to form a connector member assembly. Each connector member has front and rear faces and longitudinal elongated holes. The front and rear faces and the holes inner surface are then metal coated and metal platable and non-platable regions are formed on the front and rear surfaces. The platable regions are subjected to second metal coating forming a conductive pattern. The first metal coating is then removed from the non-platable regions to form non-conductive pattern. Each connector member is then detached from the connector assembly and first and second metal coating is removed from a portion of each side face to form a side face conductive pattern.
USE - For manufacture of connectors used for mounting electric parts such as integrated circuits, capacitors or resistors, and electrically connecting the electric part to a circuit board.
ADVANTAGE - Plurality of connectors can be manufactured simultaneously thus reducing the cost. The front, rear and side faces of the connectors have conductive and non-conductive patters.
DESCRIPTION OF DRAWING(S) - The drawing shows a flow chart of steps taken for manufacture of the connectors.
pp; 10 DwgNo 1/16
? TA
>>>No matching display code(s) found in file(s): 65

37/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012880158
WPI Acc No: 2000-051991/200004
XRAM Acc No: C00-013320
XRPX Acc No: N00-040541
Manufacturing **connectors** used for mounting electric parts such as integrated circuits
Patent Assignee: POLYPLASTICS CO INC (POPL); SANKYOUKASEI CO LTD (SANB)

Inventor: NISHIKAWA Y; YUMOTO T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5979048	A	19991109	US 95464661	A	19950621	200004	B
			US 97813893	A	19970307		

Priority Applications (No Type Date): US 97813893 A 19970307; US 95464661 A 19950621
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5979048	A		10	H01R-043/00	CIP of application US 95464661

Abstract (Basic): US 5979048 A
Abstract (Basic):

NOVELTY - The method is carried out by molding a resin to form a connector member assembly. Each connector member has front and rear faces and longitudinal elongated holes. The front and rear faces and the holes inner surface are then metal coated and metal platable and non-platable regions are formed on the front and rear surfaces. The platable regions are subjected to second metal coating forming a conductive pattern. The first metal coating is then removed from the non-platable regions to form non-conductive pattern. Each connector member is then detached from the connector assembly and first and second metal coating is removed from a portion of each side face to form a side face conductive pattern.

USE - For manufacture of connectors used for mounting electric parts such as integrated circuits, capacitors or resistors, and electrically connecting the electric part to a circuit board.

ADVANTAGE - Plurality of connectors can be manufactured simultaneously thus reducing the cost. The front, rear and side faces of the connectors have conductive and non-conductive patters.

DESCRIPTION OF DRAWING(S) - The drawing shows a flow chart of steps taken for manufacture of the connectors.

42/3,AB/1 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

2208129 NTIS Accession Number: DE2001-4504/XAB
Effect of Thick **Film** Firing Conditions on the Solderability and Structure of Au-Pt-Pd Conductor for Low-Temperature, Co-Fired Ceramic Substrates
Hernandez, C. L. ; Vianco, P. T.
Sandia National Labs., Albuquerque, NM.
Corp. Source Codes: 068123000
Sponsor: Department of Energy, Washington, DC.
Report No.: SAND98-2165C
16 Mar 1999 7p
Languages: English
Journal Announcement: USGRDR0124

Low-temperature, co-fired ceramics (LTCC) are the substrate material-of-choice for a growing number of multi-chip module (MCM) applications. Unlike the longer-standing hybrid microcircuit technology based upon alumina substrates, the manufacturability and reliability of thick **film solder** joints on LTCC substrates have not been widely studied. An investigation was undertaken to fully characterize such **solder** joints. A surface mount test vehicle with Daisy chain **electrical connections** was designed and built with Dupont(trademark) 951 tape. The Dupont(trademark) 4569 thick **film** ink (Au76-Pt21 -Pd3 wt.%) was used to establish the surface **conductor pattern**. The **conductor pattern** was fired onto the LTCC substrate in a matrix of process conditions that included: (1) double versus triple prints, (2) dielectric frame versus no frame, and (3) three firing temperatures (800 C, 875 C and 950 C). Pads were examined from the test vehicles. The porosity of the thick **film layers** was measured using quantitative image analysis in both the transverse and short transverse directions. A significant dependence on firing temperature was recorded for porosity. **Solder** paste comprised of Sn63-Pb37 powder with an RMA flux was screen **printed** onto the **circuit boards**. The appropriate components, which included chip **capacitors** of sizes 0805 up to 2225 and 50 mil pitch, leadless ceramic chip carriers having sizes of 16 I/O to 68 I/O, were then placed on the **circuit boards**. The test vehicles were oven reflowed under a N(sub 2) atmosphere. The solderability of the thick **film** pads was also observed to be sensitive to the firing conditions. Solderability appeared to degrade by the added processing steps needed for the triple print and dielectric window depositions. However, the primary factor in solderability was the firing temperature. Solderability was poorer when the firing temperature was higher.

42/3,AB/2 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

2169873 NTIS Accession Number: DE00750205/XAB
Effect of firing conditions on thick **film** microstructure and **solder** joint strength for low-temperature, co-fired ceramic substrates

Hernandez, C. L. ; Vianco, P. T. ; Rejent, J. A.
Sandia National Labs., Albuquerque, NM (US).
Corp. Source Codes: 888888888;
Sponsor: Sandia National Labs., Livermore, CA (US).; Department of Energy, Washington, DC.
Report No.: SAND99-2826C
4 Jan 2000 10p
Languages: English Document Type: Conference proceeding
Journal Announcement: USGRDR0021; NSA0028
International Brazing and Soldering Conference, Albuquerque, NM (US), 04/02/2000--04/05/2000. Sponsored by Department of Energy, Washington, DC.
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NTIS Prices: PC A02/MF A01

Low-temperature, co-fired ceramics (LTCC) are the substrate material-of-choice for a growing number of multi-chip module (MCM) applications. Unlike the longer-standing hybrid microcircuit technology based upon alumina substrates, the manufacturability and reliability of thick **film** **solder** joints on LTCC substrates have not been widely studied. An investigation was undertaken to fully characterize **solder** joints on these substrates. A surface mount test vehicle with Daisy chain **electrical** **connections** was designed and built with Dupont(trademark) 951 tape. The Dupont(trademark) 4569 thick **film** ink (Au76- Pt21-Pd3 wt.%) was used to establish the surface **conductor** **pattern**. The **conductor** **pattern** was fired onto the LTCC substrate in a matrix of processing conditions that included: (1) double versus triple prints, (2) dielectric window versus no window, and (3) three firing temperatures (800 C, 875 C and 950 C). Sn63-Pb37 **solder** paste with an RMA flux was screen **printed** onto the **circuit** **boards**. The appropriate packages, which included five sizes of chip **capacitors** and four sizes of leadless ceramic chip carriers, were placed on the **circuit** **boards** . The test vehicles were oven reflowed under a N(sub 2) atmosphere. Nonsoldered pads were removed from the test vehicles and the porosity of their thick **film** **layers** was measured using quantitative image analysis in both the transverse and short transverse directions. A significant dependence on firing temperature was recorded for porosity. The double printed substrates without a dielectric window revealed a thick **film** porosity of 31.2% at 800 C, 26.2% at 875 C and 20.4% at 950 C. In contrast, the thick **film** porosity of the triple printed substrates with a dielectric window is 24.1% at 800 C, 23.2% at 875 C and 17.6% at 950 C. These observations were compared with the shear strength of the as-fabricated chip **capacitor** **solder** joints to determine the effect of firing conditions on **solder** joint integrity. The denser **films** from the higher firing temperatures had correspondingly higher shear strengths. The 0805 chip **capacitor** had a shear strength of 12.6 (+-) 1.4 lbs. at 800 C, 13.3 (+-) 1.9 lbs. at 875 C and 13.6 (+-) 1.4 lbs. at 950 C for the triple printed substrates with a dielectric window. The trend was similar for the larger **capacitors**; the 1912's exhibiting shear strengths of 20.5 (+-) 4.8 lbs. at 800 C, 26.2 (+-) 1.7 lbs, at 875 C and 29.0 (+-) 0.2 lbs. at 950 C.

42/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007094993

WPI Acc No: 1987-094990/198714
XRPX Acc No: N87-071371
Multiple track variable resistance - uses selectively applied insulating hot melt **adhesive** and conductive binder to **connect** substrates with components and tracks
Patent Assignee: ALPS ELECTRIC CO LTD (ALPS)
Inventor: KAWANA K; OKUYA T
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3632511	A	19870402	DE 3632511	A	19860924	198714	B
US 4734672	A	19880329	US 86909490	A	19860919	198816	
DE 3632511	C	19891116				198946	

Priority Applications (No Type Date): JP 85U145077 U 19850925
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3632511	A		5		
US 4734672	A		4		

Abstract (Basic): DE 3632511 A

The **printed circuit** substrate (6) with parallel resistive tracks (7) above which sliding wipers (15) travel is carried by another substrate (1) with components (2) **attached**, and with a pattern of **connections** made of a copper **layer**. The two substrates are **connected** selectively by the insulating hot melt **adhesive** (12) and a conductive hot **sealing** binder (11).

The binder passes through holes (9) at the ends of the parallel, resistive tracks to make contact with localised contact zones (4,5) forming part of the **conductive pattern** on the lower substrate, matching their position.

ADVANTAGE - Special protective finishes are not required, there is insufficient heat to affect **soldered** joints and there are no impurities on resistive tracks.

Abstract (Equivalent): US 4734672 A

The variable **resistor circuit** module has a **printed** substrate having sliding **resistor patterns** for variable **resistor** formed by printing a thick organic **film**. A copper foil printed substrate for mounting electronic parts is laminated by insulating hot melt **adhesives**. An electroconductive heat **seal connector electrically connects** the copper foil **soldering** lands with the sliding **resistor patterns** and the **conductive** collector **patterns**.

42/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03420494
MANUFACTURE OF **PRINTED CIRCUIT BOARD**

PUB. NO.: 03-083394 [JP 3083394 A]
PUBLISHED: April 09, 1991 (19910409)
INVENTOR(s): MATSUNO YUKIO
APPLICANT(s): SHARP CORP [000504] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-219932 [JP 89219932]
FILED: August 25, 1989 (19890825)
JOURNAL: Section: E, Section No. 1084, Vol. 15, No. 258, Pg. 84, June

28, 1991 (19910628)

ABSTRACT

PURPOSE: To interconnect **conductor patterns** of both side surface of a base material without forming a copper plating **film** on the inner wall surface of a through hole by **electrically connecting** the **conductor patterns** of both side surfaces of the base material to each other by metal rods.

CONSTITUTION: After a through hole 3 is formed in a base material 1, a rod 4 made of a conductive material (e.g. brass, etc.) is engaged within the hole 3. After cream **solder** 6 is melted by an infrared ray, hot blast, etc., in a state that the lead 10a of a component (**resistor**) 10 is brought into close contact with the **solder** 6, it is cured to electrically interconnect **conductor patterns** 2 of both side surfaces of the material 1 to each other by the metal rod 4 and to **connect** the leads 10 of the component to the patterns 2. According to this method, a surface mounting both-side type **printed circuit board** can be manufactured without necessity of a plating step.

03350059

THICK **FILM CIRCUIT BOARD**

PUB. NO.: 03-012959 [JP 3012959 A]
PUBLISHED: January 21, 1991 (19910121)
INVENTOR(s): CHIKAMORI SHIGEO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-149166 [JP 89149166]
FILED: June 12, 1989 (19890612)
JOURNAL: Section: E, Section No. 1050, Vol. 15, No. 125, Pg. 143, March 27, 1991 (19910327)

ABSTRACT

PURPOSE: To set resistance of each **resistor** within an allowable region by separating as separated terminals a **conductor pattern** when **resistors** are parallely **connected** at another portion, and mutually communicating the separation terminals through electrodes of mounting parts.

CONSTITUTION: Since **conductor patterns** 12, 13 are separated by separation terminals 12a, 12b, 13a, 13b before parts 31-33 are mounted, **resistors** 21-23 printed and formed on the **conductor patterns** 12, 13 are electrically separated respectively. Accordingly, resistances of the respective **resistors** 21-23 can individually be measured. Parts 31-33 are placed on the **conductor patterns** 11-14, and one electrodes of the parts 32, 33 are **soldered** to the separating terminals 12a, 12b, 13a, 13b, whereby the separation terminals 12a, 12b, and 13a, 13b are **connected** with each other. Further, the **resistors** 21-23 are **electrically connected** in a parallel manner by **connecting** the **conductor patterns** 12, 13, and hence the circuit is constructed. Hereby, resistances of individual **resistors** can be set within an allowable range.

42/3,AB/6 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03135585
FERROMAGNETIC MAGNETORESISTANCE ELEMENT

PUB. NO.: 02-111085 [JP 2111085 A]
PUBLISHED: April 24, 1990 (19900424)
INVENTOR(s): SHIKITA YUKIHISA
APPLICANT(s): AICHI TOKEI DENKI CO LTD [350014] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-265007 [JP 88265007]
FILED: October 20, 1988 (19881020)
JOURNAL: Section: E, Section No. 952, Vol. 14, No. 328, Pg. 90, July 13, 1990 (19900713)

ABSTRACT

PURPOSE: To enable **soldering** area when **soldering** an element to a printed-wiring board to be large, prevent electrode damage due to differences in mechanical vibration and thermal coefficient of expansion, an achieve reliable **electrical connection** by providing the electrodes not only at one surface of the **printed- circuit board** but also on the side surface or rear surface.

CONSTITUTION: A **resistor pattern** 3 consisting of ferromagnetic magnetoresistance material and an electrode 4 consisting of conductive material are formed for a plurality of elements by a series operations in the thin-**film** process on a plane 2 of a plane-shaped **printed-circuit board** such as glass or ceramic and this **printed-circuit board** 1 is subjected to dicing, thus dividing into individual elements 16 to 19. After that, the thin-**film** process is executed and electrodes 4a and 4a' are provided on a side surface 5 or a rear surface 9 of the **printed-circuit board** 1. It achieves an electrode strength against burn- out and damage at a **soldered** part due to distortion caused by mechanical vibration and the difference in thermal coefficient of expansion between the **printed-circuit board** 1 and the printed-wiring board.

42/3,AB/7 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02805397
ASSEMBLY OF THICK **FILM** CIRCUIT SUBSTRATE

PUB. NO.: 01-102997 [JP 1102997 A]
PUBLISHED: April 20, 1989 (19890420)
INVENTOR(s): EBINA KIMIMASA
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-259760 [JP 87259760]
FILED: October 16, 1987 (19871016)
JOURNAL: Section: E, Section No. 797, Vol. 13, No. 344, Pg. 61, August 03, 1989 (19890803)

ABSTRACT

PURPOSE: To reduce the size of a thick **film** circuit substrate approximately to half, by laminating two thick **film circuit** substrates, **printing** a **printing** element on the opposite back

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          12356  S24
     S49       0  S45 AND S24
? S S45
     S50      36  S45
? TA
>>>No matching display code(s) found in file(s): 65

 50/3,AB/1     (Item 1 from file: 8)
DIALOG(R)File   8:Ei Compendex(R)
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01876158
  E.I. Monthly No: EIM8506-033693
   Title: FINISHING PROCESSES OF PWB'S: STUDY OF THE CHARACTERISTICS IN LAB
TESTS  AND  PERFORMANCE  COMPARISON  WITH  REGARD  TO  THE MOST SIGNIFICANT
STANDARD TESTS.
  Author: Carnovale, A.; Trucco, U.
  Corporate Source: La Zincocelere SpA, Italy
  Conference  Title:  Proceedings  -  Seminar  on  Base  Materials  and
Multilayers.
  Conference Location: Montecatini Terme, Italy   Conference Date: 19831004
  E.I. Conference No.: 06192
  Source:  Publ by European Inst of Printed Circuits, Lugano, Switz p 1. 3.
1-1. 3. 18
  Publication Year: 1983
  Language: English
  Abstract: The main function of Printed Circuit Boards (
PCB) is considered and the capacity to reliably and correctly
maintain in field electrical connections, and to support both
active and passive components. A second functional aspect,
which the user demands from the supplier is examined; this entails the P.
C. B. 's performance in the assembly phase of the finished product: a good
solderability between the terminal points of the conductive
pattern and the components mounted on it. Various characteristics of
PCB's (their finishing, coating, solderability and other
processing techniques) are discussed, with the hydro-squeegeeing judged as
the best finishing technique. Standard PCB tests are presented. 1
ref.


 50/3,AB/2     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004  Thomson Derwent. All rts. reserv.

015996624
WPI Acc No: 2004-154474/200415
XRPX Acc No: N04-123455
  Multilayer circuit board for electric components e.g.
  condenser, has conductive pattern that is electrically
  connected to conductive compound provided in trench of
  thermoplastic resin film
Patent Assignee: DENSO CORP (NPDE  ); NIPPONDENSO CO LTD (NPDE  ); KATAOKA
  R (KATA-I); KONDO K (KOND-I); MASUDA G (MASU-I)
Inventor: KATAOKA R; KONDO K; MASUDA G
Number of Countries: 005  Number of Patents: 005
Patent Family:
Patent No     Kind   Date    Applicat No    Kind   Date     Week
US 20030222340  A1  20031204  US 2003437041   A   20030514  200415  B
DE 10323903    A1  20031211  DE 1023903      A   20030526  200415
JP 2003347748  A   20031205  JP 2002158041   A   20020530  200415
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CN 1468048 A 20040114 CN 2003138342 A 20030527 200423
KR 2003093986 A 20031211 KR 200333800 A 20030527 200425

Priority Applications (No Type Date): JP 2002158041 A 20020530
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030222340 A1 7 H01L-023/53
DE 10323903 A1 H05K-001/02
JP 2003347748 A 6 H05K-003/46
CN 1468048 A H05K-001/02
KR 2003093986 A H05K-003/46

Abstract (Basic): US 20030222340 A1
Abstract (Basic):
NOVELTY - A conductive compound (51) is located in a trench provided at a **thermoplastic resin film**. A **conductive pattern** (22) which is located above the trench, is **electrically connected** to the **conductive** compound. The **conductive pattern** and **conductive** compound form a wire which has higher current carrying capacity than the **conductive pattern**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of **multilayer circuit board**.
USE - **Multilayer circuit board** used for electric components such as condenser and **resistor**.
ADVANTAGE - Provides increased current carrying capacity without thickening the **conductive pattern**.
DESCRIPTION OF DRAWING(S) - The figure shows a cross- sectional diagram explaining manufacturing method of the **multilayer circuit board**.
conductive pattern (22)
metallic **conductive pattern** (22a)
conductive compound (51)
multilayer circuit board (100)
pp; 7 DwgNo 1E/2

50/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015710176
WPI Acc No: 2003-772376/200373
XRPX Acc No: N03-618850
Ceramic laminated **circuit board** manufacturing method involves performing press **sticking** joining of frame like ceramic green sheet laminate which has opening, and primary ceramic green sheet laminate
Patent Assignee: HITACHI METALS LTD (HITK)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 2003243830 A 20030829 JP 200241557 A 20020219 200373 B

Priority Applications (No Type Date): JP 200241557 A 20020219
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 2003243830 A 6 H05K-003/46

Abstract (Basic): JP 2003243830 A
Abstract (Basic):

NOVELTY - Multiple ceramic green sheets (20e-20i) are laminated to form a primary laminate such that sheets are separated by preset distance through carrier **film**. The **conductive patterns** (7) are transferred to surface of carrier **film**. A frame like laminate which contains the ceramic green sheets (20a-20d) and a center opening, is press stuck with primary laminate such that the opening corresponds to **conductive patterns**.

USE - For manufacturing ceramic laminated **circuit board** mounted with electronic components such as transistor, FET, diode, integrated chip, resistant element, **capacitor** element, and inductor element.

ADVANTAGE - By stacking arrangement of ceramic green sheets, the **electrical connection** between circuit elements is reliably performed.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of ceramic laminated **circuit board**. (Drawing includes non-English language text).

conductive pattern (7)

ceramic green sheets (20a-20i)

pp; 6 DwgNo 1/6

50/3,AB/4 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015317665

WPI Acc No: 2003-378600/200336

Substrate for semiconductor package having patterned passive device

Patent Assignee: AMKOR TECHNOLOGY KOREA INC (AMKO-N)

Inventor: HA S H; LEE G U; OH G S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2003006510	A	20030123	KR 200142310	A	20010713	200336	B

Priority Applications (No Type Date): KR 200142310 A 20010713

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2003006510	A		1	H01L-023/52	

Abstract (Basic): KR 2003006510 A

Abstract (Basic):

NOVELTY - A substrate for a semiconductor package having a patterned passive device is provided to simplify a process and miniaturize a **printed circuit board** by forming a **conductive** passive **pattern** in the substrate without installing a passive device like a **capacitor** or inductor in the substrate in which a semiconductor chip is settled.

DETAILED DESCRIPTION - A semiconductor chip(4) is mounted on a chip mounting unit. At least two **conductive patterns**(8) **connect** an **electrical** signal of the semiconductor chip to the outside, **connected** to a **connection** pad of the semiconductor chip. A part of the **conductive pattern** extends to form a device pattern(100). The device pattern is formed in at least the same **layer** as the **conductive pattern**.

pp; 1 DwgNo 1/10

50/3,AB/5 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014410257
WPI Acc No: 2002-230960/200229
XRPX Acc No: N02-177719
Ceramic heater for wafer heating apparatus, has **resistor** with trim **pattern** having **resistance** value within three times the resistance value of portion surrounding trim pattern
Patent Assignee: KYOCERA CORP (KYOC)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001244059	A	20010907	JP 200050975	A	20000228	200229	B

Priority Applications (No Type Date): JP 200050975 A 20000228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001244059	A		11	H05B-003/20	

Abstract (Basic): JP 2001244059 A
Abstract (Basic):
NOVELTY - A heat **resistor** (5) on the main surface of a plate-shaped ceramic object, is **connected** to an **electric** supply section. The heat **resistor** includes a trim **pattern** (14), such that the **resistance** value of trim **pattern** is within three times the value of resistance in surrounding portion of the pattern.
USE - In wafer heating apparatus used for heating wafers like semiconductor wafer, liquid crystal substrate or **circuit board** to form a resist **film**.
ADVANTAGE - A wafer heating apparatus with favorable endurance is obtained by adjusting laser trimming conditions in the heat **resistor**.
DESCRIPTION OF DRAWING(S) - The figure shows the top view and sectional view explaining laser trimming of heat **resistor** in the wafer heating apparatus.
Heat **resistor** (5)
Trim pattern (14)
pp; 11 DwgNo 6/11

50/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403649
WPI Acc No: 2002-224352/200228
Related WPI Acc No: 2002-215890; 2002-225942
XRAM Acc No: C02-068431
XRPX Acc No: N02-171817
Spring structure for use in probe cards, includes conductive release material portion **attached** to anchor portion of spring metal finger for locating that release portion in between anchor portion and substrate
Patent Assignee: XEROX CORP (XERO)
Inventor: FORK D K; HO J H; LAU R K; LU J P; HO J; LU J
Number of Countries: 027 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6290510	B1	20010918	US 2000626936	A	20000727	200228	B

EP 1176635 A2 20020130 EP 2001305899 A 20010709 200228

Priority Applications (No Type Date): US 2000626936 A 20000727
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6290510 B1 14 H01R-009/09
EP 1176635 A2 E H01L-021/48
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): US 6290510 B1
Abstract (Basic):
NOVELTY - A spring structure comprises a substrate (301), a conductive release material portion (312), and a spring metal finger (320-1F) having an anchor portion **attached** to the release material pad such that the release material portion is located between the anchor portion (322) and the substrate. The spring metal finger also has a free portion (325) extending over the substrate.
USE - For use in probe cards, for electrically bonding integrated **circuits**, **circuit boards**, and electrode arrays, and for producing other devices e.g. inductors, variable **capacitors**, and actuated mirrors.
ADVANTAGE - The self-aligned release material to the spring metal finger minimizes spacing between adjacent spring structures, thus facilitating wider and stronger spring structures.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the inventive spring structure.
substrate (301)
contact pad (305)
conductive release material portion (312)
spring metal finger (320-1F)
anchor portion (322)
free portion (325)
pp; 14 DwgNo 3G/9

50/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014162834
WPI Acc No: 2001-647062/200174
XRPX Acc No: N01-483423
Analog liquid level sensor for liquid level measurement system has float assembly with contact for **connection** to graduation of metallized pattern of **printed circuit** to vary resistance between terminals
Patent Assignee: NARTRON CORP (NART-N)
Inventor: CESTERNINO K; STROM P H
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6269695 B1 20010807 US 9835712 A 19980305 200174 B

Priority Applications (No Type Date): US 9835712 A 19980305
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6269695 B1 11 G01F-023/36

Abstract (Basic): US 6269695 B1

Abstract (Basic):

NOVELTY - A float assembly has a button contact supported in a hollow buoyant housing for **electrical connection** with graduations of the metallized pattern of a **printed circuit** to change an effective resistance between the terminals (7). The terminals output an electrical signal corresponding to a contact vertical position. A resistance-to-float displacement profile is matched to the depth of a container.

DETAILED DESCRIPTION - The **printed circuit** on the support bar (3) is **electrically connected** between two spaced terminals. The **printed circuit** has an effective resistance that varies at different position between the terminals. The **printed circuit** includes a **resistor pattern** (5) and a metallized pattern (6) formed on opposite sides of the support bar for reduced electrical noise characteristics and improved hysteresis. The float assembly (21) is **connected** to a support bar to reciprocate at a vertical direction relative to the support bar in response to the level of liquid in a container.

USE - For use in liquid level measurement system used in e.g. fuel tank of motorcycle.

ADVANTAGE - Attains reduction of production cost due to simplified assembly since small number of components can be utilized because of sturdy design. Reduces contamination of component due to integral and surface additives. Improves design flexibilities for float assembly shape and size, mounting configuration and mounting location. Enables simple insertion and removal to and from container. Has improved accuracy and stability due to metallization strips of **printed circuit**. Attains reduction of noise attributed to electric and magnetic fields by using steel substrate acting as ground plane for **film resistor**.

DESCRIPTION OF DRAWING(S) - The figure shows the front view of analog liquid level sensor.

Support bar (3)
Resistor pattern (5)
Metallized pattern (6)
Terminals (7)
Float assembly (21)
pp; 11 DwgNo 1a/5

50/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013262694
WPI Acc No: 2000-434599/200038
XRAM Acc No: C00-132386
XRPX Acc No: N00-324639

Capacitor for **circuit board**, has electroconductive paste that includes titanium powder, titanium oxide powder, titanium whisker, is mixed with synthetic **resin** to form electrically **conductive film pattern**

Patent Assignee: HOKURIKU DENKI KOGYO KK (HOKU-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000150301	A	20000530	JP 98325037	A	19981116	200038	B

Priority Applications (No Type Date): JP 98325037 A 19981116
Patent Details:

Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 2000150301 A   6 H01G-004/33

Abstract (Basic): JP 2000150301 A
Abstract (Basic):
NOVELTY - The **capacitor** (5) which include an upper electrode (11), is formed on a circuit pattern (3) which consists of metallic foil, formed on the insulated substrate. The electrically conductive **film** (7) which consists of titanium is formed on the lower electrode (3a) included in circuit pattern. A PZT crystal **film** (9) which is formed on **film** (7) by hydrothermal synthesis, is **electrically connected** to the circuit pattern. An electroconductive paste which includes titanium powder, titanium oxide powder and titanium whisker is mixed with synthetic **resin** to form an electrically **conductive film pattern.**
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the **capacitor** manufacturing method.
USE - For **circuit board.**
ADVANTAGE - Since the electrically conductive **film** has characteristics that does not change, when immersed in alkali solution during hydrothermal synthesis, peeling off from lower electrode is avoided.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **circuit board** with **capacitor.**
Insulating substrate (1)
Circuit patterns (3)
Capacitor (5)
Electrically conductive **film** (7)
pp; 6 DwgNo 1/1

50/3,AB/9   (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013107403
WPI Acc No: 2000-279274/200024
XRPX Acc No: N00-210617
Flexible double sided **printed circuit board** for **capacitor** mounting, has double folding at edge to enable **electrical connection** of circuit pattern and electrode pattern which are formed at different surfaces
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
JP 2000077796 A   20000314 JP 98248913   A   1998090   200024 B

Priority Applications (No Type Date): JP 98248913 A 19980903
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 2000077796 A   10 H05K-001/02

Abstract (Basic): JP 2000077796 A
Abstract (Basic):
NOVELTY - Conductive **layers** are formed on both sides of flexible insulated **film** (2). Electrode pattern (7) is formed on conductive **layer** on one surface of insulating **film.** Edge of flexible double sided **PCB** (1) is folded twice so that conductive **layer** is inserted inwardly. An **electric** conduction material

(8) **connects** electrode pattern and a circuit **pattern** (3) formed on **conductive layer** of other surface of **film** (2).

USE - For mounting **capacitor.**

ADVANTAGE - Since **electric connection** between two conductive **layers** formed at different surfaces is enabled without using through-hole or jumper wire, simple and inexpensive **circuit board** is materialized and mechanical strength is raised.

DESCRIPTION OF DRAWING(S) - The figure shows the model sectional view of the flexible double sided **printed circuit board.**

Printed circuit board (1)
Insulated **film** (2)
Circuit pattern (3)
Electrode pattern (7)
Conduction material (8)
pp; 10 DwgNo 1/11

50/3,AB/10 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012800404
WPI Acc No: 1999-606634/199952
Related WPI Acc No: 1998-548150; 2000-278885; 2000-278886; 2000-669049
XRPX Acc No: N99-447693

Variable **resistor** arrangement structure for flyback transformer of television - has supporting pieces whose edges penetrate core line, when pulling power is applied by supported edge of core line

Patent Assignee: HOKURIKU DENKI KOGYO KK (HOKU-N)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11265811	A	19990928	JP 9862758	A	19860528	199952 B
			JP 98317705	A	19860528	
JP 3323141	B2	20020909	JP 9862758	A	19860528	200264
			JP 98317705	A	19860528	

Priority Applications (No Type Date): JP 9862758 A 19860528; JP 98317705 A 19860528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11265811	A		7	H01C-013/00	Div ex application JP 9862758
JP 3323141	B2		7	H01C-013/00	Div ex application JP 9862758
					Previous Publ. patent JP 11265811

Abstract (Basic): JP 11265811 A

NOVELTY - The lead wire support (4) has supporting pieces arranged at equal intervals which supports the edge of the core line of the lead wire inserted from the lead wire insertion holes (3b,3c). The supporting pieces has edges penetrating the core line, when pulling power is applied by supported edge of core line. DETAILED DESCRIPTION - The **resistor** circuit **pattern** having variable **resistance** body is provided on the surface of **circuit board** which is contained inside an insulated case (1). A slider is provided between insulated case and the surface of the **circuit board.** The opening of the insulated case is filled with insulated **resin** and an insulated **resin layer** (6) is formed on backside of the **circuit board.** Lead wire for output is

inserted via insertion holes (3b,3c) into side walls (1c,1i) of the insulated case. Lead wire support (4) which is **electrically connected** to the output electrode of the **resistor circuit pattern** on **circuit board** (5) is arranged between insulated case (1) and the **circuit board.**

USE - For flyback transformer of television.

ADVANTAGE - Since the supporting pieces are provided at equal intervals, stable supporting power can be maintained using few number of supporting pieces. Length of lead wire can be kept constant irrespective of the type of model, hence versatility becomes high.

DESCRIPTION OF DRAWING(S) - The figure shows the fragmentary sectional view of the variable **resistor.** (1) Insulated case; (1c,1i) Side walls of case; (3b,3c) Insertion holes; (4) Lead wire support; (5) **Circuit board;** (6) Insulated **resin layer.**

Dwg.1/10

50/3,AB/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012790884
WPI Acc No: 1999-597111/199951
XRPX Acc No: N99-441388

Electrically **conductive pattern** in **multilayered printed circuit** - is divided into discontinuous portion which is **connected** to **capacitor** mounted in position near signal line of signal **layer**

Patent Assignee: CANON KK (CANO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11261238	A	19990924	JP 9863472	A	19980313	199951	B

Priority Applications (No Type Date): JP 9863472 A 19980313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11261238	A		11	H05K-003/46	

Abstract (Basic): JP 11261238 A

NOVELTY - An electrically **conductive pattern** is divided into discontinuous portion along the direction where power supply **layer** (13) crosses signal line of signal **layer** (12). The bypass **capacitor** is mounted in the position near the signal line of signal **layer** (12), traversing the discontinuous portion of **conductive pattern** and is **connected** to the **electrically conductive pattern.** DETAILED DESCRIPTION - The electronic component which outputs high frequency signal, is **connected** to power supply **layer** (13), ground **layer** (14) and signal **layer** (15). A clock signal pattern (5') through which high frequency current flows is formed on signal **layer** (12). The power supply **layer** (13) is provided to the sub **layer** of signal **layer** (12). The ground **layer** (14) which offers standard potential to the electronic component, is provided to the sublayer of power supply **layer.** The signal **layer** (15) is provided beneath the ground **layer.** An INDEPENDENT CLAIM is also included for **multilayered printed circuit.**

USE - In **multilayered printed circuit** on which electromagnetic compatible electronic component is mounted, for use in

electronic device.
ADVANTAGE - By **connecting** the **electrically conductive pattern** to the **capacitor** generation of unnecessary radiation noise proportional to loop area formed by high frequency current and return current is suppressed. DESCRIPTION OF DRAWING(S) - The figure shows top view of **multilayered printed circuit**. (5') Clock signal pattern; (12,15) Signal **layers**; (13) Power supply **layer**; (14) Ground **layer**.
Dwg.1/9

50/3,AB/12 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012353704
WPI Acc No: 1999-159811/199914
XRPX Acc No: N99-116407
Electronic component mounting structure of **multilayer** wiring board - exposes two different **layers** of circuit pattern on upper and lower sides, on which circuit components are mounted in interconnecting manner
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11017339	A	19990122	JP 97170024	A	19970626	199914	B

Priority Applications (No Type Date): JP 97170024 A 19970626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11017339	A		10	H05K-003/46	

Abstract (Basic): JP 11017339 A
NOVELTY - Several step-like recesses are formed, from the peripheral portion towards the central section of the wiring board (11). The insulated board and conductor board laminated alternately, are etched to form circuit **patterns**. **Conductive** holes formed in insulated board for **electrically connecting** several circuit patterns. Two different **layers** of circuit pattern on upper and lower sides are exposed, on which circuit components (12) are mounted.
USE - For mounting electronic components such as **resistor**, **capacitor**, semiconductor devices on wiring board.
ADVANTAGE - Circuit components can be mounted in the wiring board in different **layers** of the step like recess, thus reducing wiring length and enabling high density mounting. Characteristic degradation of circuit, and conduction loss can be prevented. **Secures** size and weight reduction. DESCRIPTION OF DRAWING(S) - The figure shows the perspective view of **multilayer** wiring board with step-like recess. (11) Wiring **board**; (12) **Circuit** component.
Dwg.1/11

50/3,AB/13 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012136350
WPI Acc No: 1998-553262/199847

XRPX Acc No: N98-432017
Resistive pattern printing method for **PCB** - involves interposing pair of heat resistant preflux **film** between respective circuit wirings and electrical resistance body
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10247769	A	19980914	JP 9748981	A	19970304	199847	B

Priority Applications (No Type Date): JP 9748981 A 19970304
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10247769	A		6	H05K-001/16	

Abstract (Basic): JP 10247769 A
The method involves forming a pair of circuit wirings (14A,14B) made of copper laminate on an insulating substrate (12). An electrical resistance body (22) is formed above the circuit wirings using a resistive paste.
The **electrical** resistance body **connects** the circuit wirings **electrically**. A pair of heat resistant preflux **films** (20A,20B) is interposed respectively between the two circuit wirings and the electrical resistance body.
ADVANTAGE - Improves quality, reliability and product yield. Improves ion-resistant migration characteristics of circuit wiring.
Dwg.1/4

50/3,AB/14 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011676545
WPI Acc No: 1998-093454/199809
XRPX Acc No: N98-074686
Double sided **multilayered printed circuit** for mounting electronic **component** e.g. LSI, **passive component** used in electronic device - includes wiring pattern formed on both sides of substrate and predetermined parts of wiring pattern are electrically contacted to conductive **resin** composition
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU); MATSUSHITA ELECTRIC IND CO LTD (MATU)
Inventor: NAKATANI S
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9321399	A	19971212	JP 96134023	A	19960529	199809	B
US 5888627	A	19990330	US 97865055	A	19970529	199920	
JP 3197213	B2	20010813	JP 96134023	A	19960529	200148	

Priority Applications (No Type Date): JP 96134023 A 19960529
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9321399	A		11	H05K-001/03	
US 5888627	A			B32B-009/00	
JP 3197213	B2		10	H05K-001/03	Previous Publ. patent JP 9321399

Abstract (Basic): JP 9321399 A
The **printed circuit** includes a sheet substrate (100)

which is made of an organic non-woven fabrics material with density more than 0.8g/cm3. An insulating **resin** composition **layer** (101) is provided on both sides of the substrate respectively. A cover **film** (102) covers the insulating **resin** composition **layers** respectively. A through hole (103) is formed at predetermined positions of the substrate. A conductive **resin** composition (104) is filled up into the through holes.

Wiring patterns (106) formed on both sides of the substrate at predetermined positions and predetermined parts of the wiring pattern are **electrically connected** to the conductive **resin** composition.

ADVANTAGE - Improves reliability. Offers reliable **printed circuit**. Avoids influence on wiring pattern due to organic non-woven fabric material thereby enables to contact insulating **resin layer** firmly. Reduces twisting of substrate. Provides stable **connection** between wiring **pattern** and **conductive resin** composition. Improves electric insulating withstand breakdown voltage, greatly. Simplifies manufacturing process.

Dwg.1/4

50/3,AB/15 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011049426
WPI Acc No: 1997-027350/199703
XRPX Acc No: N97-023115

Printed wiring board for **electrical connection** of electronic components e.g. integrated circuit, **resistor** - has hole formed in one surface of conductor **film** that includes **print** patterns of suitable **circuits**, which branched through hole in some holes on other surface of conductor **film**

Patent Assignee: CANON KK (CANO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8288609	A	19961101	JP 9595039	A	19950420	199703	B

Priority Applications (No Type Date): JP 9595039 A 19950420
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8288609	A		6	H05K-001/11	

Abstract (Basic): JP 8288609 A

The printed wiring board has one wiring **layer** (1) and suitable **circuits** with **print patterns** with **conductor films** (2,3). An inner wall is covered by the conductor **films**.

A hole formed in one surface of the conductor **film** branched through holes (7) in some holes to the other surface of the conductor **film**.

ADVANTAGE - Improves installation efficiency of printed wiring board which can use limited area effectively, since branched through hole used in some holes and suitable print patterns are **connected**. Eliminates required print pattern for relay.

Dwg.1/6

50/3,AB/16 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010049642
WPI Acc No: 1994-317353/199439
XRPX Acc No: N94-249169
Laminated **circuit board** allowing selective setting of constants of circuit elements - has mutually insulated terminal patterns formed on **connection** wiring **layers** and selectively interconnected
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: ABE M; MISHIRO H; TAKADA R; TSUBONE K
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9422281	A1	19940929	WO 94JP327	A	19940228	199439 B
JP 6520864	X	19950511	JP 94520864	A	19940228	199527
			WO 94JP327	A	19940228	
US 5910755	A	19990608	WO 94JP327	A	19940228	199930
			US 94331506	A	19941020	
			US 96662959	A	19960613	
			US 97959711	A	19971028	

Priority Applications (No Type Date): JP 93141647 A 19930614; JP 9360295 A 19930319
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9422281	A1	J	60	H05K-003/46	
Designated States (National): JP US					
JP 6520864	X		1	H05K-003/46	Based on patent WO 9422281
US 5910755	A			H03H-007/075	Cont of application WO 94JP327
					Cont of application US 94331506
					Cont of application US 96662959

Abstract (Basic): WO 9422281 A

The laminated **circuit board** has wiring **layers** (11-1m) which comprise **conductive patterns** formed on the insulating **layer**. A **connection** wiring **layer** (2) is formed at the surface of the wiring **layers**. On the **connection** wiring **layers**, mutually insulated terminal patterns (21-2n, 20) are formed, at least two of which are **electrically connected** to the corresponding wiring **layers** by vias (P1-Pn). The terminal patterns are selectively interconnected.

The wiring **layer** may be used as laminated **capacitor** electrodes. Pref. the wiring **layer** forming the electrodes is made up of a number of independent electrodes and common electrodes. **Resistive patterns** may be formed in a series arrangement, with parallel **connection** to the corresp. wiring **layers**. Coils and inductive elements may be included to form LC filters. Wire bonding or jumper chip techniques may be used for conductive **connections**.

USE - For circuit whose constants are set by selective **connection** of circuit elements among wiring **layers**, or for circuit having required distributed circuit constants using double screening **layer** with interposed hf wiring **layer**.

Dwg.1/23

50/3,AB/17 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009727003
WPI Acc No: 1994-006853/199401
XRPX Acc No: N94-005632
Resistance unit for motor speed control in automobile air conditioner - **connects** each of lead frames to corresponding one of **resistors** by receiving end portion into fingers of fork type head part of frame
Patent Assignee: LEE W Y (LEEW-I)
Inventor: LEE W Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5274351	A	19931228	US 92878670	A	19920505	199401	B

Priority Applications (No Type Date): KR 92U3915 U 19920311
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5274351	A		9	H01C-013/00	

Abstract (Basic): US 5274351 A
The resistance unit comprises a main portion having a metallic flat substrate and an insulating **layer coated** on the surface of the main portion. A resistance circuit has a number of **resistors electrically connected** in series, the resistance **circuit** formed by **printing** a predetermined **pattern** of the **resistors** on both surfaces of the main portion, the **pattern** of **resistors** on one of the surface being electrically insulated from the pattern on the other.
A mounting device is integrally formed with and projecting outwardly from an edge of the main portion. Each of the **resistors** is printed so as to form two **layers**.
ADVANTAGE - Is durable.
Dwg.1/8

50/3,AB/18 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008346200
WPI Acc No: 1990-233201/199031
XRAM Acc No: C90-100679
XRPX Acc No: N90-180835
Resonant tag for identification etc. - has resonant thin **film** circuits having different resonant frequencies
Patent Assignee: TOKAI METALS CO (TOKA-N); TOKAI ELECTRONICS CO LTD (TOKA-N)
Inventor: MATSUMOTO T; SUZUKI Y
Number of Countries: 016 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 380426	A	19900801	EP 90400226	A	19900125	199031	B
JP 2195491	A	19900802				199119	
US 5119070	A	19920602	US 90469168	A	19900124	199225	
			US 91774158	A	19911015		
US 5201988	A	19930413	US 90469168	A	19900124	199317	
			US 91774158	A	19911015		

			US 91795677	A	19911121		
EP 380426	B1	19950823	EP 90400226	A	19900125	199538	
DE 69021743	E	19950928	DE 621743	A	19900125	199544	
			EP 90400226	A	19900125		

Priority Applications (No Type Date): JP 8914149 A 19890125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 380426	A				
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 5119070	A		14	G08B-013/22	Cont of application US 90469168
US 5201988	A		14	B44C-001/22	Cont of application US 90469168 Div ex application US 91774158 Div ex patent US 5119070
EP 380426	B1	E	17	H01F-041/04	
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU NL SE					
DE 69021743	E			H01F-041/04	Based on patent EP 380426

Abstract (Basic): EP 380426 A

Resonant tag has at least two resonant circuits having different resonant frequencies, each circuit formed of a **conductive pattern** on each side of a thin insulating **film**.The first pattern (4) includes an inductor element and an element of a **capacitor** (a) which corresponds to the resonant frequency, and the second pattern (10) contains the other element (10) of the **capacitor** facing the first, the two patterns forming anLC circuit having an inherent resonant frequency.

USE/ADVANTAGE - In identifying goods, packages etc. and also as **security** to prevent theft etc. Small, thin-**film** tag can provide a combination of two or more resonant frequencies for easy identification.

Dwg.4/18

Abstract (Equivalent): EP 380426 B

A resonant tag on which at least two **printed circuits** having different resonant frequencies are formed so as to enable said tag to be identified by the resonant frequencies of the resonant circuits, said resonant circuits comprising a first **conductive pattern** (4) formed on one surface of an insulating thin **film** (1) and a second **conductive pattern** (9) formed on the other surface of said insulating thin **film** (1), said first **conductive pattern** containing an inductor element and an element (6) of a **capacitor** which correspond to a resonant frequency of said resonant circuit, said second **conductive pattern** (9) containing the other element (10) of said **capacitor** which corresponds to said resonant frequency, said **capacitor** element (10) of said second **conductive pattern** (9) being disposed at a position where it faces said **capacitor** element (6) of said first **conductive pattern** (4) formed on one surface of said insulating thin **film**, and said two **conductive patterns** (4, 9) forming an LC resonant circuit having a given resonant frequency, characterised in that said first and second **conductive patterns** are **electrically connected** to each other at respective terminal portions (5, 11) contained in each pattern, and in that reinforcing islands are printed on each lateral side of the part of the second **conductive pattern connecting** the second capacitive element (10) and its corresponding terminal portion (11), said part crossing the coil in the inductor element of the first **conductive pattern** (4), said inductor element of each resonant circuit having a unique combination of turns, width of conductor and separation

between conductors to define a specific resonance frequency such that each resonant circuit is resonant to a different frequency, in that said capacitive element is located radially outside said inductive element, and in that each of said unique resonant circuits is separated from the other resonant circuits by a conductive separating element around said resonant circuits.

(Dwg.4/18

Abstract (Equivalent): US 5201988 A

A resonant tag is mfd. by (a) **coating** a **film** on two surfaces of an insulating **film**, (b) printing corresp. **conductive patterns** on each thin **film** using an anti-etching ink, the 1st pattern contg. an inductor and **capacitor** element corresp. to a distinct resonant frequency and the 2nd pattern contg. another **capacitor** element corresp. to the distinct resonant frequency, each 2nd **capacitor** element being at a position where it faces the corresp. **capacitor** element of the 1st **pattern**, (c) etching the **conductive films** to remove the non-printed portion and (d) forming LC resonant circuits by selectively **electrically connecting** the one and the other **capacitor** elements of at least two of the 1st and 2nd **conductive patterns**.

USE/ADVANTAGE - Used for parcels etc. The destination address does not have to be checked manually, and the parcel can be in any orientation as opposed to bar code readers where a bar code must be in a state where it can be easily optically read. The resonant frequencies are such that the tag can be identified in 2 power n ways (n = number of resonant circuits).

Dwg.4/18

US 5119070 A

Resonant tag for labelling parcels, etc. has at least two resonant circuits formed on it, with different resonant frequencies. Inductor circuits (4) are formed on an insulating substrate (1), separated from adjacent circuits by a separating portion, to reduce interference. Circuits are formed of conductive metal foil. The inductor pattern is formed on one surface of the **film** and a **capacitor** circuit pattern is formed on the other surface, the two patterns forming the resonant circuit. The tag can be identified by the combination of resonant frequencies. ADVANTAGE - Ease of checking, does not require parcel to be turned for viewing.

50/3,AB/19 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

008077145

WPI Acc No: 1989-342257/198947

XRPX Acc No: N89-260511

PCB with IC chips for memory card - has insulating substrate with islands supporting electronic modules containing memory chips and conductive paths

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: HONGU A; OHUCHI M; SAITO M; YAMADA H

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2629666	A	19891006	FR 89715	A	19890120	198947	B
JP 1251778	A	19891006				198947	
US 5018051	A	19910521	US 88291252	A	19881228	199123	
KR 9206329	B1	19920803	KR 894185	A	19890331	199404	

Priority Applications (No Type Date): JP 8878716 A 19880331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2629666	A		16		
KR 9206329	B1			G06K-019/07	

Abstract (Basic): FR 2629666 A

The **pcb** (10) includes a rectangular substrate (12), made of an insulating **resin**, and provided with several metallic terminals (14) for external **connections**. The substrate surface presents rectangular islands (16), each supporting an electronic module (18) or a DC current source (19), which are fixed in an insulating **resin** (20). The substrate is then covered by a protective **layer** (24) on top of which a **conductive pattern** (26) is formed. **Connections** to the module terminals (22) are made via through holes (28) performed in the **layer**.

A second insulating **layer** (30) covers the whole structure. Each electronic module includes several memory chips (34) mounted in an insulating **resin**, and interconnected by conductive paths formed on top of an insulating **layer** which protects the module.

ADVANTAGE - Accommodates increased number of chips, in more compact and thinner structure. Has higher storage capacity with fast access to records.

1/3

Abstract (Equivalent): US 5018051 A

The IC card comprises a card-shaped main substrate having a surface on which recess portions are formed and an edge portion having a **connector layer** with an external **connector** terminal pattern formed on it. Circuit modules are embedded in the recess portions in main substrate. Each module has electronic components including IC chips, a chip **capacitor** and a thin D.C. battery unit, and a double-**layered** wiring structure for providing **electric connection** between the electronic components and the **connector** terminal pattern.

The double-**layered** wiring structure comprises a first wiring **layer** formed on the main substrate to cover the circuit modules and a second wiring **layer** formed insulatively above the former wiring **layer**. The first wiring **layer** has a first wiring pattern that extends in a first direction of the main substrate to be coupled to the electronic components. The second wiring **layer** has a second wiring pattern that extends in a second direction of the main substrate to be coupled to the first wiring pattern and the **connector** terminal pattern.

ADVANTAGE - Effective mounting of increased number of IC chips. Compact, thin card. (7pp

50/3,AB/20 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007943128
WPI Acc No: 1989-208240/198929
XRPX Acc No: N89-158812

Tape automated bonding package for semiconductor chip - has decoupling **capacitors connected** to ground and power leads positioned adjacent chip

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: FRANKENY R F; RAKES J M

Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 324244	A	19890719	EP 88311767	A	19881213	198929 B
JP 1181540	A	19890719	JP 88289037	A	19881117	198935
US 4903113	A	19900220	US 88145808	A	19880115	199014
EP 324244	B1	19941130	EP 88311767	A	19881213	199501
DE 3852291	G	19950112	DE 3852291	A	19881213	199507
			EP 88311767	A	19881213	

Priority Applications (No Type Date): US 88145808 A 19880115
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 324244	A	E	8		
Designated States (Regional): DE FR GB					
US 4903113	A		7		
EP 324244	B1	E	8	H01L-023/64	
Designated States (Regional): DE FR GB					
DE 3852291	G			H01L-023/64	Based on patent EP 324244

Abstract (Basic): EP 324244 A

The tape automated bonding package comprises an electrically insulating **polymer layer**, and a pattern of electrical leads on the **layer**, including signal, ground and power leads, for interconnecting the semiconductor chip to a **printed circuit** substrate. A decoupling **capacitor** is directly **connected** to a ground and to a power lead on the **polymer layer**.

The semiconductor chip is rectangular and includes a ground and a power lead positioned on the **layer** as a pair of adjacent leads passing to a corner area on the chip, said decoupling **capacitor** being **connected** to the leads in the pair at a position adjacent the corner areas of the chip.

ADVANTAGE - Easily automated for mass production.

2/4

Abstract (Equivalent): EP 324244 B

A tape automated bonding package for a semiconductor chip comprising a semiconductor chip (70,95) mounted on an electrically insulating **polymer layer** (64), and a pattern of electrical leads on the **layer**, including signal (26), ground (62,78) and power (60,76) leads for interconnecting the semiconductor chip (70) to a **printed circuit** substrate, characterised by a surface mounted decoupling **capacitor** (52,54,56,58,80,90) directly **connected** to a ground (62,78) and to a power (60,76) lead on the **polymer layer** (64), so that the **capacitor** is supported by the **polymer layer**, wherein the **capacitor** lies on the side of the **layer** (64) opposite to the chip and at least partially within an area of the **polymer layer** defined by the footprint (8) of the chip and in which said **layer** (64) includes a plurality of apertures (72,74,84) for passing leads on the side of the **layer** defined by a footprint (8) of the chip, through to **connections** on the chip, two of said apertures (72,74) **connecting** ground and power leads in said area to the underside of the chip, said **capacitor** (52,54,56,58,80,90) being **connected** directly to said ground and power leads in said area.

(Dwg.1/7

Abstract (Equivalent): US 4903113 A

The semiconductor device TAB package for **electrical connection** to **printed circuit** substrate, has conductive planes comprising a planar flexible insulating member, a **pattern** of **conductive** leads, including power and ground

leads, formed on the flexible insulating member and a decoupling **capacitor** across adjacent one of the power and ground leads. Another device **connects** the semiconductor device to first ends of some **conductive** leads in the **pattern**. The device comprises apertures in the flexible insulating member adapted for permitting direct **attachment** of the power and ground leads to interior sites on a surface of the semiconductor device or on peripheral edges of the' device.

Another device selectively **connectss** opposite ends of some of the conductive leads to surface circuitry and internal conductive planes of the circuit substrate.

ADVANTAGE - Enhanced performance characteristics. (7pp

50/3,AB/21 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007790439
WPI Acc No: 1989-055551/198908
XRAM Acc No: C89-024526
XRPX Acc No: N89-042319
Miniaturised electronic part with moulded **resin** casing - formed around **resin** flexible board having **conductor patterns**
Patent Assignee: TEIKOKU TSUSHIN KOGYO KK (TEIK-N)
Inventor: INAGAKI J; KAKU Y; KIKUCHI N; MIZUNO S; MORITA K; YAGI N; KIKUCHI N K
Number of Countries: 008 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 304112	A	19890222	EP 88201651	A	19880729	198908 B
JP 1050504	A	19890227	JP 87207433	A	19870821	198914
JP 1081204	A	19890327	JP 87238448	A	19870922	198918
JP 1166505	A	19890630	JP 87325679	A	19871222	198932
US 4928082	A	19900522	US 88234946	A	19880822	199024
US 4935718	A	19900619	US 88234952	A	19880822	199027
US 4978491	A	19901218	US 88244165	A	19880913	199102
US 5071611	A	19911210	US 89447441	A	19891207	199201
EP 304112	B1	19931006	EP 88201651	A	19880729	199340
DE 3884718	G	19931111	DE 3884718	A	19880729	199346
			EP 88201651	A	19880729	

Priority Applications (No Type Date): JP 87325679 A 19871222; JP 87207433 A 19870821; JP 87238448 A 19870922; JP 87224239 A 19870907; JP 87238449 A 19870922
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 304112	A	E	30		
Designated States (Regional): DE FR GB IT NL SE					
EP 304112	B1	E	33	H05K-005/00	
Designated States (Regional): DE FR GB IT NL SE					
DE 3884718	G			H05K-005/00	Based on patent EP 304112

Abstract (Basic): EP 304112 A
Electronic part is fabricated having a moulded **resin** casing (1) housing a flexible board (3) made from synthetic **resin film** on which are formed electric **conductor patterns** (3-1,3-2,3-3,3-4) slidingly contacted by slider contacts of the part. Metallic terminal pieces (2-1 to 2-5) are joined to upper surface end portions of the electric **conductor pattern** and a

securing resin film, the same substance as the flexible board, is placed upon them, a terminal portion being provided by locally fusing **securing film** and board **film** together. The flexible board is inserted into the **resin** casing such that predetermined portions of the metallic terminal pieces project to the outside and the electric **conductor patterns** are exposed to its interior only, board and casing being integrated.

USE/ADVANTAGE - Electronic part is a rotary or sliding type variable **resistor** or code switch having greatly reduced size and thickness.

Abstract (Equivalent): EP 307977 B

A moulded **resin** casing of an electronic part equipped with a flat cable (12,62,75), the casing interiorly accommodating a flexible board (3,53,73) on which are formed electric **conductor patterns** (3-1, 3-2, 3-3, 3-4, 53-1, 53-2, 73-1, 73-2) slidingly contacted by contacts of a slider (5-2) of the electronic part, wherein said flexible board comprises a synthetic **resin film** and the electric **conductor patterns** formed on said synthetic **resin film**; said flexible board is formed integral with the flat cable comprising the synthetic **resin film** on which are formed further electric **conductor patterns** (12-1, 12-2, 12-3, 12-4, 12-5, 62-1, 75-1) **electrically connected** to said electr

Abstract (Equivalent): US 5071611 A

Process for mfg. a moulded synthetic **resin** casing of an electronic part with an integrally **attached** flexible flat cable comprises prepg. a first die which is brought into close contact with a flexible board including a **resin film** on which a number of electric conductor panels are formed with a groove formed around the die periphery. The centre of the die surface has a hole for forming a support with a second die opposed to it forming a recess corresp. to the part of the first die including the die surface and part of the groove.

The board is clamped with the **attached** cable between the two dies to cause the patterned surface to abut the die. The recess is filled between the dies with molten **resin** by injection from a central portion. The board is of a material and thickness causing it to be folded back to allow **resin** to fill the hole to hold it.

USE - For **circuit boards**. (27pp)t

US 4978491 A

A process for mfg. a **molded synthetic resin** casing of an electronic prod. comprises prepn. of a die having a flat surface which is brought into close contact with a surface of a flexible board including a **resin film** having electrical **conductor patterns** on it.

A support forming hole is provided in a central portion of the flat surface and a groove is provided around the surface periphery for forming a side portion of the casing. A second die is disposed opposite to the first and has a casing bottom forming a recess corresp. to the flat surface and the groove.

The board is clamped between the two dies to cause the **conductor patterns** to a butt the flat surface and edge of the first die to lie inside the outer edge of the groove. A cavity between the two dies is filled with a molten **resin** material from a central portion of the recess of the second die. The injection is carried out at a pressure such that the board is punctured and the **resin** fills the support forming hole of the first die.

ADVANTAGE - A redn. in size of electronic components is provided. (27pp)g

US 4935718 A

Rotary or sliding electronic part has a moulded **resin** casing in which a flexible board is received. **Conductor patterns** are formed on the board and are contacted by a slider. The patterns are formed on a synthetic **resin film** and are exposed to the exterior of the casing. Metallic terminal pieces are **secured** to the ends of the patterns.

ADVANTAGE - Reduced size. (27pp)

US 4928082 A

A device, partic. a rotary or sliding type variable **resistor** or code switch, comprises a moulded **resin** casing (91) contg. an integrally **attached** flexible board (93) including a **plastic film** with an electrical **conductor pattern,** with an electronic part slidable on the board to cooperate with the pattern. The casing is moulded onto the board and is oriented so that the pattern is exposed.

A flexible flat cable (92) is integrally **attached** to the board extending away from the casing and includes a **plastic film** with a second **conductor pattern** directly **connected** to the first pattern. The first pattern is pref. exposed to the inner bottom and side of the casing.

ADVANTAGE - Reduces size and thickness and eliminates the need to **connect** a cable to the electronic part. (27pp)o

50/3,AB/22 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007073469
WPI Acc No: 1987-073466/198711
XRPX Acc No: N87-055679
High frequency filter for portable radio transmitter - has inductive pins passing through tips of wedge shaped planar **capacitor** sections
Patent Assignee: BOSCH GMBH ROBERT (BOSC)
Inventor: BOTTCHER R; FRANKE M; WAIZENEGG D
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3531531	A	19870312	DE 3531531	A	19850904	198711	B
EP 214492	A	19870318				198711	
EP 214492	B	19911127				199148	
DE 3682636	G	19920109				199203	

Priority Applications (No Type Date): DE 3531531 A 19850904
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3531531	A		4		
EP 214492	A				
Designated States (Regional): CH DE FR LI SE					
EP 214492	B				
Designated States (Regional): CH DE FR LI SE					

Abstract (Basic): DE 3531531 A

The space saving multiple way filter of bushing type has a **printed circuit board** carrying components both sides, supported by pins inside a housing between top and base sheets. The base sheet (13) carries a **film** or plate (18) of insulating material with a **pattern** of **conductive** zones through which the pins (16) pass, **electrically connected** to them, and then protruding from the bottom to form contact pins. The conductive

zones form a planar **capacitor**, and the pins also act as inductances for the filter.

The conductive zones (22 to 29) are triangular (23,24;27,28) or have triangular portions (22,25,26,29), and the pins are positioned to pass through their pointed tips along two sides of the housing. Each line of pins passes through a contact strip under the housing.

USE/ADVANTAGE - Filter can be used in hand held radio transmitters where space is limited.

Dwg.2/5

Abstract (Equivalent): EP 214492 B

High-frequency lead-through filter for lines which are lead through a conductive housing wall, characterised in that the lead-through filter (36) is formed by a **capacitor** in strip conductor technology and the inductor is formed by a lead-through line (16) which is lead in an insulated manner through the housing wall (13) and penetrates through the **capacitor**. (6pp)

50/3,AB/23 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003467877
WPI Acc No: 1982-15821E/198208
Resonant tag circuit - comprising capacitative and inductive coatings on opposite surfaces of **plastics** carrier strip
Patent Assignee: VANDEBULT J (VAND-I)
Inventor: VANDEBULT J
Number of Countries: 010 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8200541	A	19820218				198208	B
EP 59723	A	19820915	EP 81902204	A	19810731	198238	
US 4369557	A	19830125				198306	
EP 59723	B	19860326				198613	
DE 3174181	G	19860430				198619	

Priority Applications (No Type Date): US 80176061 A 19800806
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8200541	A	E	41		
Designated States (National): DE GB NL SE US					
Designated States (Regional): AT CH DE FR GB LU NL SE					
EP 59723	A	E			
Designated States (Regional): AT CH DE FR GB LI LU NL SE					
EP 59723	B	E			
Designated States (Regional): DE FR GB NL SE					

Abstract (Basic): WO 8200541 A

A resonant tag having a tuned circuit is made by forming on one surface of a **plastics** carrier strip a **pattern** of **conductive coating** material defining a first area serving as a **capacitor** plate and a second area sewing as an inductor, and applying a **layer** of conductive **coating** to the other surface of the strip, at least part of the **layer** being located opposite the **capacitor** defining area to define a second **capacitor** plate. Finally a **connection** is made through the strip to **connect** the end of the inductor defining area to the locating **layer** on the opposite side. The coatings may be formed by applying a metal foil, or the like, and etching away areas to leave the

desired pattern.

Repetitive patterns may be produced upon a continuous carrier strip and the strip subdivided into individual tags

Abstract (Equivalent): EP 59723 B

A method of fabricating a plurality of individual planar resonant tags, each tag having at least one self-contained operative tuned circuit with integrally formed circuit elements including an inductor and a **capacitor**, the method comprising the steps of providing an insulative substrate web (10) of material of predetermined thickness and dielectric characteristics and having first and second faces and a conductive surface with an etchant-resistive material a first repetitive circuit **pattern** defining a first **conductive** area (14) serving as a first plate of said **capacitor** and an inductor (16) **electrically connected** at a first end thereof to said first conductive area; etching said conductive surface to remove unprinted portions of said conductive surface thereby to provide a first repetitive **conductive** circuit **pattern** (12) conforming to said **printed circuit** pattern; applying a **layer** (20) of conductive material to said second web face in a second repetitive circuit pattern, said second repetitive circuit **pattern** defining a second **conductive** area in at least partial alignment with said first conductive area and serving as a second plate of said **capacitor**, the web serving as a dielectric of the **capacitor**, and a conductive strip effecting **electrical connection** between said second conductive area and a second end of said inductor; and separating said web between adjacent said first repetitive circuit patterns to provide individual planar resonant tags. (22pp)

50/3,AB/24 (Item 23 from file: 350)

DIALOG(R)File 350:Derwent WPIX

001990160

WPI Acc No: 1978-03172A/197802

Printed circuit plate with high wiring concentration - having circuit element **films** inserted between flexible insulating **layer**, having **conductive** copper **patterns** and nonflexible substrate

Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 52140867	A	19771124				197802	B
JP 83057920	B	19831222				198404	

Priority Applications (No Type Date): JP 7658585 A 19760520

Abstract (Basic): JP 52140867 A

Plate is mfd. by (1) adhering a flexible sheet having an electric insulating **layer** of a bonding agent and electroconductive patterns of copper foil on the insulating **layer** to a non-flexible substrate; (2) inserting circuit element **films** (e.g. **resistor**, dielectrics, conductor **films**, etc.) formed on the insulating **layer** between the non-flexible substrate and the flexible sheet; and (3) **electrically connecting** the circuit element **films** to the electroconductive patterns on the flexible sheet by an electroconductive paint which is applied to holes which penetrate the flexible sheet.

The circuit elements are freely disposed, and the wiring concn. of the electroconductive patterns to the surface is increased.

The flexible sheet is obtd. by **coating** a **thermosetting resin adhesive** agent of epoxy **resin** and polybutadiene **resin** on the back of a copper foil. The circuit elements comprise a **resistor** (e.g. carbon powder-phenol **resin** paint), a conductor (e.g. Ag powder-epoxy **resin** paint) and a dielectrics (e.g. polysulphone **resin**, barium titanate powder-epoxy **resin** paints, etc.). The non-flexible sheet comprises a paper substrate and a phenol **resin** sheet.

50/3,AB/25 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06713406
MULTILAYERED CIRCUIT BOARD

PUB. NO.: 2000-299241 [JP 2000299241 A]
PUBLISHED: October 24, 2000 (20001024)
INVENTOR(s): AZUMA KOJI
OBARA YOZO
APPLICANT(s): HOKURIKU ELECTRIC IND CO LTD
APPL. NO.: 11-105363 [JP 99105363]
FILED: April 13, 1999 (19990413)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a **multilayered circuit board**, where **circuit boards** are easily, surely and **electrically connected** together, when a chip electronic component is mounted on an inner **circuit board**.

SOLUTION: A **multilayered circuit board** is manufactured in a manner where a first circuit pattern 15 is formed on the surface of a first **circuit board** 11, a second **circuit** pattern 13 is formed on the rear of a second **circuit board** 10, and the second **circuit board** 10 is laminated on the first **circuit board** 11 through the intermediary of an insulating **layer** 12 of prepreg. A chip **capacitor** 1 is equipped with electrodes 5 and 6, which are each formed on its rear and front, and the **capacitor** 1 is arranged on the first **circuit board** 11 so as to **electrically connect** the electrode 6 formed on its rear to the first circuit **pattern** 15. A **conductive** projection 14 is provided to the second circuit pattern 13 to come into contact with the electrode 5 formed on the front of the **capacitor** 1, penetrating through the insulating **layer** 12. The first circuit pattern 15 and the second circuit pattern 13 are **electrically connected** through the intermediary of the chip **capacitor** 1.

50/3,AB/26 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06126782
MULTI-LAYER CIRCUIT BOARD AND MANUFACTURE THEREFOR

PUB. NO.: 11-068319 [JP 11068319 A]
PUBLISHED: March 09, 1999 (19990309)
INVENTOR(s): HORIUCHI MICHIO
MURAMATSU SHIGEJI
APPLICANT(s): SHINKO ELECTRIC IND CO LTD
APPL. NO.: 09-216176 [JP 97216176]
FILED: August 11, 1997 (19970811)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **multi-layer circuit board** capable of the decoupling of a power supply line or the like without providing a chip **capacitor** or the like in the **multi-layer circuit board** of **resin** obtained by a build-up method.

SOLUTION: For this board, plural one-sided metallic foil **films** for which metallic foil is **adhered** to one surface of a **resin film** composed of **thermosetting resin** are laminated and formed on both surfaces of a core substrate 12 and respective **conductor patterns** 18a-e and 20a-e formed from the metallic foil are held among **resin layers** 14a-d and 16a-d composed of the **resin film** and **electrically connected** by via holes 24 passed through the **resin layers** 14a-d and 16a-d. In this case, the **resin layers** 14c and 16c and the core substrate 12 for forming the **multi-layer circuit board** 10 held between the **conductor pattern** for the power supply line and the **conductor pattern** for a ground line are formed by the **resin** to which dielectric material powder whose dielectric constant at 1 MHz is equal to or more than 100 is mixed.

50/3,AB/27 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06062549
PRINTED CIRCUIT BOARD AND MANUFACTURE THEREOF

PUB. NO.: 11-004057 [JP 11004057 A]
PUBLISHED: January 06, 1999 (19990106)
INVENTOR(s): ONOZUKA KAZUKO
MASATOKI TAMIJI
KAI IKUYO
KONISHI MASAMI
APPLICANT(s): SONY CORP
APPL. NO.: 09-155547 [JP 97155547]
FILED: June 12, 1997 (19970612)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **printed** resistance **circuit board** and a method for manufacturing the same, which is able to prevent the surfaces of copper foils, which constitute a **circuit pattern** of a printed **resistance circuit board** from being oxidized, and to prevent ion migration between the copper foils which are **connected** via an **electric resistor** from being generated.

SOLUTION: In a circuit pattern, constituted of copper foils formed on an insulating substrate 10, the surfaces of first and second copper foils 12a

and 12b, which constitute a portion of the circuit **pattern** requiring an electric **resistor**, are covered with palladium skin **films** 18a and 18b formed, for example, by plating at portions other than those covered with an undercoat 16. The first copper foil 12a and the second copper foil 12b are **connected** with each other via an electric **resistor** 20, while the palladium plated **films** 18a and 18b are, respectively interposed at the portions of the first and second copper foils 12a and 12b, which are in contact with the electrical **resistor** 20.

50/3,AB/28 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05916655
FILM CAPACITOR

PUB. NO.: 10-199755 [JP 10199755 A]
PUBLISHED: July 31, 1998 (19980731)
INVENTOR(s): KAWAI WAKAHIRO
APPLICANT(s): OMRON CORP [000294] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-017821 [JP 9717821]
FILED: January 15, 1997 (19970115)

ABSTRACT

PROBLEM TO BE SOLVED: To dispense with through hole processing and a process of processing a conductive projection, by interposing interposing two pieces of **capacitors** in series between the external electrodes consisting of a pair of **conductive patterns** constituted of **thermoplastic conductive adhesives** juxtaposed on a dielectric **film**.

SOLUTION: The **conductor patterns** 4 and 5 of a thin **film capacitor** 1 are opposed to the wiring patterns 7 and 8 of a **circuit board** 6, and then they are stuck fast onto the **circuit board** 6. Next, the **thermoplastic** conductive **adhesives** constituting the **conductive patterns** 4 and 5 are fused again and are put in fluid condition by giving heat is given to the junction while applying proper pressure, thus they are put in affinity with the wiring patterns 7 and 8 on the **circuit board** 6. Then, the junction is cooled to harden the **thermoplastic adhesives** constituting the **conductive patterns** 4 and 5. Hereby, the **electric connection** between the thin **film capacitor** 1 and the **circuit board** 6 is performed, and at the same time, both are bonded firmly.

50/3,AB/29 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05440805
FREQUENCY ADJUSTMENT METHOD FOR DIELECTRIC FILTER

PUB. NO.: 09-055605 [JP 9055605 A]
PUBLISHED: February 25, 1997 (19970225)

INVENTOR(s): FURUTA ATSUSHI
NOBA TAKAYA
YOSHIDA EIKICHI
APPLICANT(s): TOKIN CORP [330203] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-207196 [JP 95207196]
FILED: August 14, 1995 (19950814)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain an adjustment method to decrease the frequency of the dielectric filter without deteriorating the Q and strength of its conductive **film**.

SOLUTION: A **conductor pattern** 22 **connecting electrically electric** coupling elements such as **capacitors** or the like and a ground **conductor pattern** 23a or the like **connecting** two dielectric coaxial resonators 11a, 11b to ground are formed on a **printed circuit board** 21. As shown in a caption A in the Figure, epoxy **resin** is fixed as a capacitive inclusion to cover the ground **conductor pattern** 23a and the **conductor pattern** 22 to which a terminal pin 27 is **connected**. In the case of fixing the epoxy **resin** with a specific dielectric constant εof 5 by an amount of 3.3μl, it is confirmed that the resonance frequency is decreased by about 1MHz.

50/3,AB/30 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

05412608
HIGH VOLTAGE VARIABLE **RESISTOR**

PUB. NO.: 09-027408 [JP 9027408 A]
PUBLISHED: January 28, 1997 (19970128)
INVENTOR(s): TSUNEZAWA ICHIRO
BANDO SHIGERU
APPLICANT(s): HOKURIKU ELECTRIC IND CO LTD [327816] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-183269 [JP 96183269]
FILED: July 12, 1996 (19960712)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a high voltage variable **resistor** which makes it possible to **connect** a lead wire in the final stage of assembling and to retain the core wire of the lead wire **filmly** by a lead wire pinching means.

SOLUTION: A lead wire pinching means 4, which is **electrically connected** to the **resistor** circuit **pattern** on a **circuit board**, is arranged between an insulating case 1 and a **circuit board** 5. The lead wire pinching means 4 has a plurality of clamp pieces which clamp the end part of the core wire of the lead wire, inserted from the lead wire inserting hole provided on the insulating case 1. The lead wire insulating hole is composed of a large diameter part 3a, which permits the insertion of the insulating-**coated** part of the lead wire with one end opened toward outside, a tapered part 3b which is extending continuously with the other end of the large diameter part 3a with the diameter becoming smaller in the direction of insertion of the lead wire, and a small diameter part 3c which opens into the insulating

case 1 in continuity with the tapered part 3b and extends toward the lead wire pinching means 4.

50/3,AB/31 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

04830080
HYBRID INTEGRATED CIRCUIT DEVICE

PUB. NO.: 07-122680 [JP 7122680 A]
PUBLISHED: May 12, 1995 (19950512)
INVENTOR(s): YAMAMOTO TOMOHIKO
KOKUZEN SHIYOUICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-188530 [JP 94188530]
FILED: August 10, 1994 (19940810)

ABSTRACT

PURPOSE: To enhance the heat dissipation properties by dissipating the heat directly from the rear of an insulating board and to enhance the mechanical strength of the insulating board while facilitating the assemblage.

CONSTITUTION: A circuit pattern 2 of a thick **film** copper wiring, for example, is formed on the surface of an insulating **board** 1. The **circuit** pattern includes a terminal pattern 8 **connected electrically** with a terminal pattern 81 formed on the rear through holes 7. Active elements, e.g. transistors and ICs, and passive elements, e.g. **resistors** and **capacitors**, are fixed to the surface of the insulating board and **connected electrically** with the circuit **pattern**. A **conductive pattern**, e.g. a thick **film** copper wiring and a thick **film** silver-platinum wiring, is formed on the rear of the insulating board as well as the terminal pattern 81. It is employed for grounding and **connected electrically** with the active and passive elements to be grounded, fixed to the surface of the board, through the through holes made appropriately through the **conductive pattern** . The through holes are normally made immediately under the element but it is preferably spaced apart slightly from the element when the element is transistor.

50/3,AB/32 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

04153510
CIRCUIT BOARD WITH INDUCTANCE ELEMENT

PUB. NO.: 05-145210 [JP 5145210 A]
PUBLISHED: June 11, 1993 (19930611)
INVENTOR(s): HASHIMA AKIRA
YAMAKAWA MITSUAKI
SAKAMOTO KAZUNORI
APPLICANT(s): TOSHIBA LIGHTING & TECHNOL CORP [461465] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-031176 [JP 9131176]
FILED: February 27, 1991 (19910227)
JOURNAL: Section: E, Section No. 1437, Vol. 17, No. 528, Pg. 125,

September 22, 1993 (19930922)

ABSTRACT

PURPOSE: To obtain a **circuit board** with inductance element suitable for constituting a high-frequency mounting circuit device, etc., by **electrically connecting** a **conductor pattern film** formed in a chip-shaped core with the **conductor pattern film** of a **circuit board** body.

CONSTITUTION: A **circuit board** body is constituted when a required circuit **pattern** 4a, a **resistor** and a plurality of streaks of **conductor pattern films** 5a forming a part of inductance coil are printed and baked on a principal plane. These **conductor pattern films** 5a are formed almost parallel to each other. On the other hand, a ceramic core chip 5b, in which a plurality of streaks of **conductor pattern films** 5c constituting a required inductance coil at the time of arrangement and **connection** with the **conductor pattern films** 5a are formed on the peripheral face, is provided on the region of the **conductor pattern films** 5a. Then, after this ceramic core chip 5b is arranged on the region forming the **conductor pattern films** 5a, the **conductor pattern films** 5c are **electrically connected** in the manner of corresponding to the **conductor pattern films** 5a so that a desired inductance coil is constituted.

50/3,AB/33 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03902217
LAYERED CERAMIC **CAPACITOR**

PUB. NO.: 04-267317 [JP 4267317 A]
PUBLISHED: September 22, 1992 (19920922)
INVENTOR(s): HANYA MASASHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-028389 [JP 9128389]
FILED: February 22, 1991 (19910222)
JOURNAL: Section: E, Section No. 1315, Vol. 17, No. 57, Pg. 143, February 04, 1993 (19930204)

ABSTRACT

PURPOSE: To improve mounting density and provide **layered** ceramic **capacitors** with a structure to prevent the occurrence of unnecessary capacitance during mounting in **layered** ceramic **capacitors** used for all kinds of electronic equipment.

CONSTITUTION: The structure consists of dielectric **layers** 7 and internal electrodes 8, which are alternately **layered** , and two terminal electrodes 9a and 9b, which are **connected electrically** to the end face of the above mentioned internal electrodes 8 on the same side. Because the terminal electrodes 9 and 9b are placed on the same side, it is possible to mount the **layered** ceramic **capacitor** using the end with the smallest area as the mounting surface and the mounting density can be improved without shrinking the main body. In addition, because it is possible to mount the **layered** ceramic **capacitor** so that the internal electrode is vertical to the **conductive pattern** on the

circuit board during mounting, the occurrence of unnecessary capacitance can be avoided.

50/3,AB/34 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

03191287
THICK **FILM CIRCUIT BOARD**

PUB. NO.: 02-166787 [JP 2166787 A]
PUBLISHED: June 27, 1990 (19900627)
INVENTOR(s): CHIKAMORI SHIGEO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-322345 [JP 88322345]
FILED: December 21, 1988 (19881221)
JOURNAL: Section: E, Section No. 978, Vol. 14, No. 429, Pg. 113, September 14, 1990 (19900914)

ABSTRACT

PURPOSE: To obtain a thick **film circuit board** in which a predetermined resistance value can be easily obtained by suppressing variation in an area resistance by composing a gold conductor **film** between a **conductor pattern** and a **resistor pattern**.

CONSTITUTION: A **conductor pattern** 2 is formed in a predetermined pattern of silver-palladium alloy on the surface of an insulating board 1 made of alumina, etc., and a gold conductor **film** 4 is formed previously at a position formed with a **resistor**. A **resistance pattern** 3 is so formed by printing of ruthenium oxide as to superpose partly on the gold conductor **film** 4, and the **resistance pattern** 3 is **electrically connected** to the **conductor pattern** 2 through the gold conductor **film** 4. Accordingly, since the gold conductor **film** 3 having high chemical stability and extremely small diffusion coefficient is interposed between the **conductor pattern** 2 and the **resistance pattern** 3, intermetallic molecule bond is not generated between the **conductor pattern** 2 and the **resistance pattern** 3 even by heat treating in a **layer** baking step. As a result, the intermetallic molecule bond between the **resistance pattern** and the gold **conductor film** is suppressed to easily and stably obtain a predetermined resistance value.

50/3,AB/35 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

02078259
INTEGRATED CIRCUIT PACKAGE

PUB. NO.: 61-292359 [JP 61292359 A]
PUBLISHED: December 23, 1986 (19861223)
INVENTOR(s): TAKAHASHI YUTAKA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-134478 [JP 85134478]

FILED: June 20, 1985 (19850620)
JOURNAL: Section: E, Section No. 508, Vol. 11, No. 154, Pg. 109, May 19, 1987 (19870519)

ABSTRACT

PURPOSE: To realize a logic circuit having high mounting density, and high performance of high noise margin by providing an input/output terminal **electrically connected** with an IC chip terminal, a **resistor electrically connected** at one end, and an external resistance terminal **connected** with the other end of the **resistor** in an IC package.

CONSTITUTION: A leadless carrier package has a bonding pad 4 on a chip carrier base 1 of a ceramic, an input/output terminal 6 **connected** with a **conductor pattern** of a carrier base inner **layer**, a terminating **resistor** 7 of the inner **layer connected** at one end with the pad 4, and an external resistance terminal 8 **connected** with the other end of the **resistor** 7. The chip pad 3 of the chip 2 and the pad 4 are **electrically connected** therebetween by bonding wirings 5, and a **sealing** plate is **secured** onto the upper surface 9 of the base 1 by an **adhesive**. Further, the resistance value of the **resistor** 7 is so selected as to match the characteristic impedance of the signal line on a **printed circuit board**.

50/3,AB/36 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

01053271
THERMAL HEAD

PUB. NO.: 57-203571 [JP 57203571 A]
PUBLISHED: December 13, 1982 (19821213)
INVENTOR(s): TAGUCHI NOBUYOSHI
YAMASHITA KIYOHARU
ARAI MASAJI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-089049 [JP 8189049]
FILED: June 10, 1981 (19810610)
JOURNAL: Section: M, Section No. 199, Vol. 07, No. 59, Pg. 10, March 11, 1983 (19830311)

ABSTRACT

PURPOSE: To reduce the weight of a thermal head and to improve the heat radiating effect of the head by interposing a thermally conductive heat radiating plate between a heat resistant insulating substrate and a heat radiating base and interposing a thermoelectric insulating plate between a **multilayer circuit board** and the base.

CONSTITUTION: A heat resistant insulating substrate 2 made of glazed alumina or the like is provided through a heat radiating plate 22 having good thermal conduction such as iron series material or the like on part of a heat radiating base 21 made of aluminum or the like, and a common electrode 4, a heating **resistor** 3 and an isolating electrode 5 are provided on the substrate. A **multilayer circuit board** 11 is provided through a thermoelectric insulating plate 23 on the other art of the base 21. A semiconductor device is provided on the board 11 or between the substrate 2 and the board 11. A **coating film** 8 is

preferably formed on the lower surface of the device 7. A **conductive pattern** 24 is formed on the back surface of the board 11, and the pattern 24 is preferably **electrically connected** to a signal line 12 through a through hole 25.

55/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4627625 INSPEC Abstract Number: B9405-2210B-002
Title: SMT on flex circuits
Author(s): Woznicki, T.
Author Affiliation: Flex Circuit Design Co., San Jose, CA, USA
Journal: Printed Circuit Design vol.10, no.9 p.14, 16-17
Publication Date: Sept. 1993 Country of Publication: USA
CODEN: PCIDEU ISSN: 0884-9862
Language: English
Abstract: It surprises many engineers to discover that components can be put on flex circuits. The fact is that ICs, capacitors, resistors, switches, sensors and all sorts of components are put on flex circuits - and not just multilayer or rigid-flex circuits but single-layer flex circuits too. The author discusses the differences between flex circuits and rigid boards, and how to design flex circuits to accept SMT devices. The fabrication process for flex circuits is similar to making rigid boards; a copper laminate is printed and etched to create the circuit pattern. The main difference is that rigid uses a stiff, **fiberglass** core material and flex does not. To place an SMT device on a flex, simply **drill** or punch **holes** in the coverfilm so it exposes the copper where you need to **solder** . Then place a stiffner underneath the component area to support the **solder** joints.
Subfile: B

55/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013991137
WPI Acc No: 2001-475352/200151
XRAM Acc No: C01-142478
XRPX Acc No: N01-351866
Multi-layer rigid-flex printed circuit board has photo-imageable **solder** mask applied to exposed region of conductive layer to allow photodefinition of openings upon conductive layers
Patent Assignee: CARON A R (CARO-I); JEAN S L (JEAN-I); KEATING J E (KEAT-I); LARMOUTH R S (LARM-I); MILLETTE L J (MILL-I); TELEDYNE IND INC (TDCO)
Inventor: CARON A R; JEAN S L; KEATING J E; LARMOUTH R S; MILLETTE L J
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010010303	A1	20010802	US 97800844	A	19970214	200151	B
			US 99260198	A	19990301		
US 6350387	B2	20020226	US 97800844	A	19970214	200220	
			US 99260198	A	19990301		

Priority Applications (No Type Date): US 97800844 A 19970214; US 99260198 A 19990301
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010010303	A1		9	H05K-001/00	Div ex application US 97800844
US 6350387	B2			H05K-003/46	Div ex application US 97800844

Abstract (Basic): US 20010010303 A1
Abstract (Basic):

NOVELTY - The board laminate has a base stock composite containing a flexible core formed by laminating a conductive layer (48) to a flexible insulator layer. A secondary insulator layer affixed with a conductive layer (52) is attached to the base stock such that a section of the conductive layer is exposed. A photo-imageable **solder** mask (54) applied to the exposed portion allows photodefinition of openings upon the conductive layers.

DETAILED DESCRIPTION - The secondary insulator layer and conductive layer (52) have corresponding cut regions proximate to flexible core of the base stock composite. The secondary insulator layer has an overlapping section that overlaps a section of the flexible core. The conductive layers comprise a copper sheet having dimensions of about 9 microns to 2 ounce and the flexible insulator layer comprises **fiber glass** sheet impregnated with any one of epoxy prepreg of thickness of 1.5-5.0 mils or polyimide film of thickness of 0.5-3.0 mils or combination of both. The photo-imageable **solder** mask comprises a flexible thermal curing liquid photo-imageable **solder** mask of thickness 1-3 mils. The thickness of **solder** mask is adjusted relative to that of conductive layer. The conductive layers are imaged and etched to form conductor patterns.

An INDEPENDENT CLAIM is also included for multi-layer rigid-flex circuit board preparation process which involves imaging and etching the conductive layer (48) to form conductor patterns. A conductive layer (52) is laminated to secondary insulator layer such that the conductive layer (52) contains a cover section comprising copper or insulative material. The copper section covers the flexible core section of conductive layer (48) laminated to the flexible insulator layer and is not bonded to flexible core section. The cover section forms an opening in between flexible core section and cover section. The conductive layers are laminated to form a rigid section. The cover section covering the flexible core section is removed to expose flexible core section. The exposed core section and conductive layer (50) are coated with a photo-imageable **solder** mask. The **solder** mask is formed by depositing a liquid precursor of **solder** mask by spray coating and curing the liquid precursor. The **solder** mask is coated in both rigid and flexible sections of rigid-flex printed circuit board. By drilling the rigid section of printed circuit board, holes are formed. By cleaning and plating through **drilled holes**, conductive barrels connecting conductors in conductor patterns are formed. The photodefined openings formed on conductive layers are subjected to surface coating comprising any one of tin/lead coating, gold coating or an organic coating to prevent oxidation.

USE - For fabricating multi-layer combined rigid/flex printed circuit board containing flexible **solder** mask.

ADVANTAGE - The flexible **solder** mask is cost effective. Since the flexible **solder** mask is applied on both rigid and flex sections and photodefinition of openings is allowed, the additional process steps required to fabricate the flexible inner layers are avoided.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of the rigid/flex printed circuit board.

Conductive layers (48,50,52)

Photo-imageable **solder** mask (54)

pp; 9 DwgNo 3/3

62/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5818430 INSPEC Abstract Number: B9803-2210B-004
Title: Filament-wound laminates [**PCB** materials]
Author(s): Klimpl, F.
Author Affiliation: Compositech Ltd., Hauppage, NY, USA
Journal: Printed Circuit Fabrication vol.20, no.12 p.26, 28, 30, 32-3
Publisher: Miller Freeman,
Publication Date: Dec. 1997 Country of Publication: USA
CODEN: PCFAE6 ISSN: 0274-8096
SICI: 0274-8096(199712)20:12L.26:FWLM;1-O
Material Identity Number: F904-97013
Language: English
Abstract: From four **layer** PC cards to 50-**layer** backplanes, design requirements for smaller pads, buried vias and microvias, **ball grid** arrays (BGAs), and MCM-Ls intensify the pressure on profitability in the highly competitive laminates arena. The difficulty in maintaining acceptable profit margins is evident as profit margins of publicly-held **printed circuit** companies are released. It is becoming abundantly clear that the steady appetite for "faster and denser" boards has moved beyond the currently acceptable levels of manufacturability of fabric-based laminates. This article describes new laminates which are being developed to replace conventional woven **fiber glass** /epoxy laminates. The most promising product development incorporates a method that replaces the conventional weaving loom with a computer-controlled continuous-filament winding system that offers opportunities for enhanced performance and reduced cost. Filament-wound structures in a composite offer a more efficient filament packing density and better fiber-to-**resin** stress transfer.
Subfile: B

62/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5374849 INSPEC Abstract Number: B9610-0170J-090
Title: A study of chemical decapsulation techniques for new generation **plastic** molded IC packages
Author(s): Chowdhury, R.; Adams, O.; Bartlett, J.; Todd, C.; Huynh, T.
Author Affiliation: Texas Instrum. Inc., Houston, TX, USA
Conference Title: ISTFA '95. 21st International Symposium for Testing and Failure Analysis p.281-6
Publisher: ASM Int, Materials Park, OH, USA
Publication Date: 1995 Country of Publication: USA xiii+367 pp.
ISBN: 0 87170 554 0 Material Identity Number: XX95-02134
Conference Title: Proceedings of 21st International Symposium for Testing and Failure Analysis
Conference Sponsor: ASM Int
Conference Date: 6-10 Nov. 1995 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: IC decapsulation is a crucial step for failure analysis. Improper decapsulation may lead to corrosion of bond pad metallizations and/or etching of the lead fingers, effectively precluding further functional analysis. New generation **plastic** mold compounds and

packages have rendered the traditional manual decapsulation techniques all but obsolete. This paper compares the advantages of automated decapsulation equipment and techniques over the conventional manual techniques. To encompass a majority of the decapsulation problems, we used a variety of **plastic** mold compounds and package types in this study. One **fiberglass layered ball grid** array (**BGA**) package was especially vulnerable to manual chemical decapsulation, which attacked not only bond pad metallizations, but also the **PCB** materials. We show that available spray etch systems provide reliable results with a substantial reduction in decapsulation time.
Subfile: B

62/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02098739
E.I. Monthly No: EIM8606-040611
Title: **SOLDER ATTACHMENT** OF SMD's IN A LOW VOLUME PRODUCTION ENVIRONMENT.
Author: Roffey, N. R.
Corporate Source: Honeywell, Inc, Clearwater, FL, USA
Conference Title: Proceedings of the Technical Conference - IEPS, Fourth Annual International Electronics Packaging Conference.
Conference Location: Baltimore, MD, USA Conference Date: 19841029
E.I. Conference No.: 06732
Source: Publ by Int Electronics Packaging Soc, Glen Ellyn, IL, USA p 167-180
Publication Year: 1984
Language: English
Abstract: The author addresses the **attachment** of leadless ceramic chip carriers to printed wiring boards in a low-volume environment using a minimum of automation. The printed wiring assemblies fall into two types. One PWA is a **multilayer** polyimide **fiberglass** with a copper-invar-copper laminate core. There are two different configurations of the polyimide-glass PWA. One is the central processor unit (CPU), and the other is the local memory unit (LMU). Both have approximately 144 leadless chip carriers mounted on one side of each of the boards. The other PWA is constructed of G10 epoxy-**fiberglass** and has twenty-four leadless chip carriers mounted on each side of the board. These **fiberglass** boards are dummy boards to be used in engineering thermal cycle tests. Earlier investigations and tests revealed that the most efficient method of **attachment** would involve **solder reflow** using a batch-type vapor phase machine. To support this type of **solder attachment**, a silk screening process would have to be developed as well as a rapid and accurate means of assembling the chip carriers to the printed wiring boards. Cleaning processes, as well as inspection techniques, would have to be developed.

62/3,AB/4 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02043673
E.I. Monthly No: EI8611113165
E.I. Yearly No: EI86089018
Title: IMPORTANCE OF ELECTROKINETIC POTENTIAL IN THE CATALYSIS OF

ELECTROLESS COPPER ON EPOXY-GLASSFIBRE LAMINATES.
Author: Lea, C.; Whitlaw, K. J.
Corporate Source: NPL, Teddington, Engl
Source: Transactions of the Institute of Metal Finishing v 64 pt 3 Aug 1986 p 124-128
Publication Year: 1986
CODEN: TIMFA2 ISSN: 0020-2967
Language: ENGLISH
Abstract: To obtain high quality **soldering** assembly of double-sided and **multilayer printed circuit boards**, it is advantageous that the copper barrels plated through the epoxy-**fiberglass** board should be both impervious and **adherent**. This requires the electroless copper precursor to exhibit complete and uniform coverage of the drilled laminate surface. While it is possible to achieve complete coverage by the electroless copper by using any commercially available catalyst system, consideration of the electrokinetic potential of the catalyst suggests that the stringent requirements of conditioning the substrate surface to achieve uniform deposition can be relaxed when using a positvely charged catalyst. This is because a catalyst with a positive electrokinetic potential is not repelled from the negatively charged substrate surface, whereas a catalystic system with a negative electrokinetic potential necessarily incorporates careful conditioning of the surface to achieve complete coverage. (Author abstract) 5 refs.

62/3,AB/5 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1909598 H.W. WILSON RECORD NUMBER: BAST99044860
Cool solutions
Stratford, James;
Electronics World v. 105 no1759 (July 1999) p. 604-6
DOCUMENT TYPE: Feature Article ISSN: 0959-8332

ABSTRACT: Thermal product specialist Bergquist has launched new products that replace thermally-conductive grease. The Gap Pad is a conformal material having enhanced thermal conductivity. Thermal Clad is an insulated metal substrate. Sil Pad combines a tough carrier including **fiberglass** and **silicone** rubber as a binding material. Softface is used for high-volume applications where it can withstand **solder** baths and cleaning equipment.

62/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016055036
WPI Acc No: 2004-212887/200420
Related WPI Acc No: 2004-106779
XRAM Acc No: C04-084383
XRPX Acc No: N04-168603
Electronic device and flexible **circuit board** assembly for organic light emitting diode displays, has Z-interconnections each for coupling device electrical contact to corresponding **circuit board** electrical contact
Patent Assignee: PALANISAMY P (PALA-I)
Inventor: PALANISAMY P
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040016568	A1	20040129	US 2002379456	P	20020510	200420 B
			US 2003435960	A	20030512	

Priority Applications (No Type Date): US 2002379456 P 20020510; US 2003435960 A 20030512

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040016568	A1		18	H05K-003/34	Provisional application US 2002379456

Abstract (Basic): US 20040016568 A1

Abstract (Basic):

NOVELTY - An electronic device and flexible **circuit board** assembly includes an electronic device including a substrate, electronic components, and device electrical contacts; flexible **circuit board** including flexible substrate and **circuit board** electrical contacts; and Z-interconnections each for coupling the device electrical contact to a corresponding **circuit board** electrical contact.

DETAILED DESCRIPTION - An electronic device and flexible **circuit board** assembly includes an electronic device (100) including a substrate (300) having a back surface, electronic components (302) coupled to the substrate, and device electrical contacts (112) coupled to the back surface of the substrate and to the electronic components; flexible **circuit board** (102) including a flexible substrate (118) having front and back surfaces, and **circuit board** electrical contacts (116) coupled to the front surface of the corresponding to the device electrical contacts; and Z-interconnections (114) each for coupling the device electrical contact to a corresponding **circuit board** electrical contact.

An INDEPENDENT CLAIM is also included for manufacturing an electronic device by providing the electronic device and flexible **circuit board**; forming conductive bumps on the electronic device or flexible **circuit board**, preferably on the device electrical contact or corresponding **circuit board** electrical contact; aligning the electrical contacts of the electronic device and **circuit board**; pressing the electronic device and the flexible **circuit board** together such that the conductive bumps spans the gap between each device electrical contact and the corresponding **circuit board** electrical contact; and curing the conductive bumps to form Z-interconnections.

USE - Used as electronic device and **circuit board** assembly for organic light emitting diode displays.

ADVANTAGE - The assembly involves low cost **circuit board** materials and has high yields and long-term reliability electrical **connections**.

DESCRIPTION OF DRAWING(S) - The figure is a cut-away view of flexible **circuit board**.

Electronic device (100)
Circuit board (102)
Device electrical contacts (112)
Z-interconnections (114)
Circuit board electrical contacts (116)
Flexible substrate (118)
Substrate (300)
Electronic components (302)
pp; 18 DwgNo 3B/8

62/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015901644
WPI Acc No: 2004-059484/200406
Related WPI Acc No: 2002-546516
XRAM Acc No: C04-024461
XRPX Acc No: N04-048116

Electronic package, for **connection** of e.g. integrated circuit chips to chip carriers, comprises reformable ball positioned on contact pad of substrate and elastic collar or sleeve positioned around the reformable ball

Patent Assignee: ALCOE D J (ALCO-I)
Inventor: ALCOE D J

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030196826	A1	20031023	US 99300783	A	19990427	200406 B
			US 2003402289	A	20030328	

Priority Applications (No Type Date): US 99300783 A 19990427; US 2003402289 A 20030328
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030196826	A1		31	H01L-023/02	Div ex application US 99300783 Div ex patent US 6583354

Abstract (Basic): US 20030196826 A1
Abstract (Basic):

NOVELTY - An electronic package comprises:

(a) a substrate (603) having a contact pad (605A, 605B);

(b) a reformable ball (607A) positioned on the contact pad; and

(c) an elastic collar or sleeve (609A) positioned around the reformable ball.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) making an electronic package comprising providing a substrate having a contact pad; positioning a reformable ball on the contact pad: positioning an elastic collar or sleeve around the reformable ball, the elastic collar or sleeve exerting a girdling force on the reformable ball; and softening the reformable ball such that the elastic collar or sleeve elongates the reformable ball; and

(b) an apparatus for positioning an elastic collar or sleeve around the reformable ball, comprising a first plate having a pin projecting into the opening of the elastic member; a second plate having an aperture and interposed between the first plate and the elastic collar or sleeve.

The pin projects through the aperture in the second plate. The second plate is movably positioned with respect to the pin of the first plate for removing the elastic collar or sleeve from the pin and positioning the elastic collar or sleeve around the reformable ball such that the reformable ball is located in the opening of the elastic collar or sleeve.

USE - **Connection** of integrated circuit chips to chip carriers, chip carrier to **printed circuit boards**, and modules to **printed circuit** cards.

ADVANTAGE - The invention is adaptable to mass production and has an improved stand off capability to provide improved package reliability.

DESCRIPTION OF DRAWING(S) - The figure is a partial side section on a much enlarged scale of an electronic package.
Substrate (603)
Contact pad (605A, 605B)
Reformable ball (607A)
Elastic collar or sleeve (609A)
pp; 31 DwgNo 6/22

62/3,AB/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015681528
WPI Acc No: 2003-743717/200370
Related WPI Acc No: 2003-274284
XRAM Acc No: C03-204147
XRPX Acc No: N03-595591
Printed circuit board comprises first **layer**, second **layer** having surfaces, where one surface includes recessed portion, interstitial component with lead, in recessed portion, and via
Patent Assignee: KOPF D R (KOPF-I); HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: KOPF D R
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030035275	A1	20030220	US 2000579022	A	20000525	200370 B
			US 2002247369	A	20020920	
US 6704207	B2	20040309	US 2000579022	A	20000525	200418
			US 2002247369	A	20020920	

Priority Applications (No Type Date): US 2000579022 A 20000525; US 2002247369 A 20020920
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030035275	A1		8	H05K-001/00	Cont of application US 2000579022
					Cont of patent US 6480395
US 6704207	B2			H05K-007/10	Cont of application US 2000579022
					Cont of patent US 6480395

Abstract (Basic): US 20030035275 A1
Abstract (Basic):
NOVELTY - A **printed circuit board** comprises:
(a) a first **layer** having first and second surfaces;
(b) a second **layer** having a third and fourth surfaces, where one includes a recessed portion;
(c) an interstitial component, having a lead, placed in the recessed portion; and
(d) a via electrically **connecting** the first to the second **layer**, coupled to the lead of the interstitial component.
DETAILED DESCRIPTION - A **printed circuit board** comprises:
(a) a first **layer** having first and second surfaces, where the first comprises a device mounted on it;
(b) a second **layer** having a third and fourth surfaces opposed to one another, and where one of the surfaces includes a recessed portion (220, 222, 224, 228);
(c) an interstitial component (104, 106, 108, 114), having a lead, **securely** disposed in the recessed portion; and
(d) a via (206, 210) electrically **connecting** the first

layer to the second **layer**, coupled to the lead of the interstitial component.

An INDEPENDENT CLAIM is included for a method of making a **printed circuit board** as above with an interstitial component, comprising routing a portion of the second or third surfaces to form a recessed portion; placing an interstitial component in the recessed portion; and applying a **solder** paste compound to a surface-mount axial lead of the interstitial component, to couple the lead from the interstitial component to an inner trace of the **printed circuit board.**

USE - As a **printed circuit board.**

ADVANTAGE - The **printed circuit board** allows certain components to be optimally placed in relation to high-speed signal traces such that the signal perturbations and potential electromagnetic interference radiation are significantly reduced. The **printed circuit board** substrate cavity can be tuned to further enhance signal quality and reduce the number of signal vias that must traverse the **printed circuit board.**

DESCRIPTION OF DRAWING(S) - The figure shows a **multi-layer printed circuit board** having multiple interstitial components.

Interstitial component (104, 106, 108, 114)

Via (206, 210)

Recessed portion (220, 222, 224, 228)

pp; 8 DwgNo 4/4

62/3,AB/9 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015610573

WPI Acc No: 2003-672730/200364

XRAM Acc No: C03-183622

XRPX Acc No: N03-537164

Adhesive for bonding substrates for e.g. **printed circuit boards**, formed from composition comprising polyarylene ether, **thermosetting resin** and cure agent

Patent Assignee: GENERAL ELECTRIC CO (GENE)

Inventor: DAVIS M J; RIDING G H; TRACY J E; YEAGER G W

Number of Countries: 028 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1167484	A2	20020102	EP 2001305293	A	20010618	200364	B
JP 2002173659	A	20020621	JP 2001184174	A	20010619	200364	
KR 2001114177	A	20011229	KR 200135063	A	20010620	200364	

Priority Applications (No Type Date): US 2000644012 A 20000822; US 2000212752 P 20000620

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1167484	A2	E	12	C09J-171/00	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
JP 2002173659	A		40	C09J-171/10	
KR 2001114177	A			C09J-171/00	

Abstract (Basic): EP 1167484 A2

Abstract (Basic):

NOVELTY - An **adhesive** formed from a composition comprising

(for 100 weight% of **resin** portion) a polyarylene ether **resin** having a number average molecular weight of 8,000-13,000 (5-50 weight%), a **thermosetting resin** (50-90 weight%) and a cure agent (0.1-7 weight%).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(1) a laminate comprising:

(i) a **thermoplastic** substrate;

(ii) a conductive metal foil at least partially disposed on the side(s) of the substrate; and

(iii) the **adhesive** disposed between the substrate and the metal foil; and

(2) the formation of the laminate, which comprises **coating** a surface of a **thermoplastic** or metallized **thermoplastic** or conductive metal foil with the **adhesive**, and applying the **adhesive** against a first surface of a **thermoplastic** substrate.

USE - The **adhesive** composition especially used to bond **thermoplastic** substrates used in the fabrication of **printed circuit boards**, rigid flex **circuit boards** or any other articles where good dielectric properties are desired.

ADVANTAGE - Substrates bonded with the **adhesive** may be used for capable of microvia technology and can be laser drilled without interference of reinforcements such as woven or chopped **fiberglass**. Suitable bond strengths are achieved between **thermoplastic** substrate materials, conductive metals such as copper, and other **thermoset** base **circuit board** materials. The **adhesive resin** has better processability, exhibits reduced B-staged (partially cured) friability, and minimal flow during lamination.

pp; 12 DwgNo 0/0

62/3,AB/10 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015572757
WPI Acc No: 2003-634914/200360
Related WPI Acc No: 2003-352451
XRAM Acc No: C03-173441
XRPX Acc No: N03-504942

Monolithic, integrated structure comprises semiconductor integrated circuit(s) containing conductive pads, and embedded in substrate such that pads face outward and are visible along the top surface of substrate

Patent Assignee: NATHAN R J (NATH-I); SHEPHERD W H (SHEP-I)
Inventor: NATHAN R J; SHEPHERD W H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030059976	A1	20030327	US 2001963337	A	20010924	200360	B
			US 200298021	A	20020312		

Priority Applications (No Type Date): US 200298021 A 20020312; US 2001963337 A 20010924
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030059976	A1		34	H01L-021/48	CIP of application US 2001963337

Abstract (Basic): US 20030059976 A1
Abstract (Basic):

NOVELTY - A structure comprises a substrate having a top surface; and semiconductor integrated circuit(s) embedded in the substrate and containing conductive pads (43-1) on one surface. Each circuit is embedded in the substrate such that the conductive pads on the circuit face outward and are visible along the top surface.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) fabrication of a packaged semiconductor chip comprising forming a cavity (44) in the substrate (41); placing an integrated circuit chip (42) in the cavity; forming a **layer** of conductive material over the top surface (41a, 42a) of the integrated circuit chip, the electrically conductive pads and the surface of the substrate; and forming the electrically conductive material into an electrically conductive interconnect pattern interconnecting the pads to form an electrical circuit;

(b) fabrication of monolithic integrated structure containing integrated circuit chip(s) embedded in a substrate comprising placing the integrated circuit chip(s) to be embedded in the substrate in a template; pressing the template against the top surface of the substrate in which the chips are to be embedded; heating the substrate to soften the material making up the substrate; pressing the chips placed on the top surface using a planarizing plate until the surface of the chips are coplanar with that of the substrate; and allowing the substrate containing the chips to cool;

(c) fabrication of substrate comprising forming cavities having an opening in the substrate; placing integrated circuit chips in the cavities such that a visible surface of the chips is coplanar with the top surface; forming a conductive **layer** on the top surface of the substrate; and patterning the conductive **layer** to form a conductive interconnect to interconnect the integrated circuit chips into a desired circuit; and

(d) a module comprising substrates having a top surface; and integrated circuit die being embedded in the substrate.

USE - As monolithic, integrated structure.

ADVANTAGE - The invention can incorporate the functions represented by semiconductor chips fabricated using different technologies, such as analog and digital, to form one or more partial or entire electronic systems. Smaller integrated circuit chips can be fabricated, thus allowing manufacturers to place more die on a wafer and thus reducing the cost of the resulting die. The cost of the resulting package integrated circuit chip is also reduced. The invention allows standard semiconductor or **printed circuit board** processing techniques to be used to fabricate integrated circuit packages at the same time, thus further reducing the cost of each package. **Solder bumps** used for assembling flip chip packages can be eliminated. The integrated circuit chip package has electrical **connections** to the circuit chip which have lower inductance and capacitance than prior art packages, and provides a lower cost, thinner and higher performing package than in the prior art.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a **ball grid** array substrate.

Substrate (41)
Top surface (41a, 42a)
Integrated circuit chip (42)
Conductive pads (43-1)
Cavity (44)
pp; 34 DwgNo 4/21

62/3,AB/11 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015469505
WPI Acc No: 2003-531651/200350
XRAM Acc No: C03-143551
XRPX Acc No: N03-421806
Circuit board for electronic equipment such as radio and television sets, includes insulating **layer** arranged between transmission **layer** and ferrite-containing **layer**
Patent Assignee: JENSEN S (JENS-I); ANDREW CORP (ANDC)
Inventor: JENSEN S
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030062965	A1	20030403	US 2001966553	A	20010927	200350	B
US 6603080	B2	20030805	US 2001966553	A	20010927	200353	

Priority Applications (No Type Date): US 2001966553 A 20010927
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030062965	A1		14	H04B-003/28	
US 6603080	B2			H05K-001/03	

Abstract (Basic): US 20030062965 A1
Abstract (Basic):
NOVELTY - The **circuit board** (10) comprises an electrically conductive transmission **layer** (14) and a ferrite-containing **layer** (18) separated from each other. An insulating **layer** (16) is arranged between transmission **layer** and ferrite **layer.**
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **circuit board** treatment method.
USE - In wide variety of electronic equipment such as radio and television sets, remote controls, calculators, telephones, cellular telephones, personal computers, personal digital assistants, vehicles, manufacturing equipment and other applications.
ADVANTAGE - Permits effective suppression of unwanted radio frequency and microwave signals on **circuit boards.**
DESCRIPTION OF DRAWING(S) - The figure shows a cross- sectional view of **circuit board.**
Circuit board (10)
Transmission **layer** (14)
Insulating **layer** (16)
Ferrite-containing **layer** (18)
pp; 14 DwgNo 1/8

62/3,AB/12 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015367545
WPI Acc No: 2003-428483/200340
Related WPI Acc No: 2004-118869; 2004-154321
XRAM Acc No: C03-113018
XRPX Acc No: N03-342012
Fabrication of low loss **multilayer printed circuit board** involves laminating together **printed circuit board layers** by using at least one bonding ply containing **fluoropolymer** composite and **thermosetting adhesive** composition

Patent Assignee: TONOGA LTD (TONO-N); TONOGA INC (TONO-N)
Inventor: MCCARTHY T F; WYNANTS D L; MCCARTHY T
Number of Countries: 101 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6500529	B1	20021231	US 2001952486	A	20010914	200340	B
WO 200326371	A1	20030327	WO 2002US29364	A	20020916	200340	

Priority Applications (No Type Date): US 2001952486 A 20010914
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6500529	B1		15	B32B-003/00	
WO 200326371	A1	E		H05K-003/46	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 6500529 B1
Abstract (Basic):
NOVELTY - A low loss **multilayer printed circuit board** is made by providing at least one bonding ply having a **fluoropolymer** composite and a **thermosetting adhesive** composition; and laminating together **printed circuit board layers** by using the bonding ply. The composite comprises non-expanded **fluoropolymer**(s); and a substrate from woven fabrics, nonwoven fabrics or **polymeric films**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a bonding ply composition comprising a **fluoropolymer** composite **layer** comprising non-expanded **fluoropolymer**(s) and a substrate from woven fabrics, nonwoven fabrics or **polymeric films**; and an **adhesive layer** comprising a **thermosetting adhesive** composition disposed in or impregnated into the **fluoropolymer layer**.
USE - For fabricating a low loss **multilayer printed circuit board** (claimed).
ADVANTAGE - The inventive process enables **circuit board** fabricators to **connect layers** of **fluoropolymer**-based substrates together at reasonable fabrication temperatures (approximately equal to 350 degrees F/177 degrees C). The hybrid composite has the advantages of polytetrafluoroethylene (PTFE) in that it can be processed like a low temperature **thermoset**.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic of a laminate core material comprising **fiberglass**, polytetrafluoroethylene, a **thermosetting resin adhesive layer**, and copper cladding.
pp; 15 DwgNo 5/5

62/3,AB/13 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015309491
WPI Acc No: 2003-370425/200335
Related WPI Acc No: 1999-560290; 2000-655598
XRAM Acc No: C03-097970

XRPX Acc No: N03-295416
Using socket to electrically interconnect microelectronic assembly and substrate, comprises providing socket including apertures having deflectable, resilient lip regions made of dielectric material
Patent Assignee: TESSERA INC (TESS-N)
Inventor: HABA B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6493932	B1	20021217	US 98112545	A	19980709	200335 B
			US 99363496	A	19990729	
			US 2000629728	A	20000731	

Priority Applications (No Type Date): US 98112545 A 19980709; US 99363496 A 19990729; US 2000629728 A 20000731
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6493932	B1		16	H05K-003/39	Cont of application US 98112545 Cont of application US 99363496 Cont of patent US 5951305 Cont of patent US 6126455

Abstract (Basic): US 6493932 B1
Abstract (Basic):
NOVELTY - A method of using a socket to electrically interconnect a microelectronic assembly having electrically conductive joining units and a substrate having electrically conductive contacts, comprises providing socket with apertures having deflectable, resilient lip regions made of a dielectric material; positioning the socket over the substrate; and juxtaposing microelectronic assembly with substrate.
DETAILED DESCRIPTION - Using a socket to electrically interconnect a microelectronic assembly having electrically conductive joining units and a substrate having electrically conductive contacts (4), comprises:
(i) providing a socket including apertures (3) having deflectable, resilient lip regions made of a dielectric material;
(ii) positioning the socket over the substrate so that the apertures are in alignment with at least some of the electrically conductive contacts of the substrate;
(iii) juxtaposing the microelectronic assembly with the substrate so that the socket is between the microelectronic assembly and the substrate and so that the electrically conductive joining units of the microelectronic assembly confront the contacts of the substrate; and
(iv) inserting the electrically conductive joining units of the microelectronic assembly into the apertures of the socket so that the conductive joining units deflect the deflectable lip regions of the socket for allowing the joining units to pass through each aperture, where the conductive joining units of the microelectronic assembly are held in electrical contact with the contacts of the substrate by the resilience of the deflectable lip regions contacting the conductive joining units.
USE - For using a socket to electrically interconnect a microelectronic assembly and a substrate, such as a **printed circuit board** (for permanent **connection**), or test **circuit board** (for temporary **connection**, for testing purposes).
ADVANTAGE - The socket incorporates a grabbing or locking feature that is capable of capturing the joining units of the chip assembly. It is lidless because it does not require a lid or any other mechanism for applying pressure to a semiconductor chip assembly to maintain an electrical contact between the terminals of the chip assembly and the

socket.

DESCRIPTION OF DRAWING(S) - The figure is a side view of a socket in conjunction with a semiconductor chip assembly and a **printed circuit board**.

Flexible dielectric element (2)
Apertures (3)
Contacts (4)
Backing element (5)
Holes (6)
Semiconductor chip assembly (10)
Solder balls (13)
Printed circuit board (14)
pp; 16 DwgNo 5/7

62/3,AB/14 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015029966
WPI Acc No: 2003-090483/200308
XRAM Acc No: C03-022891
XRPX Acc No: N03-071459
Electronic sub assembly for passing optical signals to computers for diagnostics/analysis comprises circuit laminated substrate and conductive lead
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HALL R R; LIN H T; MAJKA C J; SEASTRAND N C; SEWARD M F; SMITH R V
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020131252	A1	20020919	US 2001811101	A	20010316	200308	B
US 6721187	B2	20040413	US 2001811101	A	20010316	200425	

Priority Applications (No Type Date): US 2001811101 A 20010316
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020131252	A1		10	H05K-007/02	
US 6721187	B2			H05K-007/02	

Abstract (Basic): US 20020131252 A1
Abstract (Basic):

NOVELTY - An electronic sub assembly comprises a circuit laminated substrate (10) having top and bottom surfaces separated by an edge surface (18a, 18b) and mounted by active/passive device(s), and a conductive lead embedded in the substrate and **connected** to the active/passive device(s).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(a) a method of making an electronic sub assembly comprising fabricating a circuit laminated substrate; providing active or passive device mounted on the top and bottom surfaces; providing active or passive device mounted on the top and bottom surfaces; mounting an active or passive device on the edge surface; embedding a conductive lead in the substrate; electrically **connecting** the conductive lead to the device on the top or bottom surface of the substrate;

(b) a **printed circuit board** having two spaced apart, parallel surfaces comprising a top surface (48) and a bottom surface; an edge surface between the top and bottom surfaces;

conductive leads embedded in the **circuit board** parallel to the top and bottom surfaces and terminating in **connection** points along the edge surface; an active or passive device mounted on the edge surface and electrically joined through the **connection** points to the conductive leads; and active or passive device mounted on the top or bottom surface electrically joined to the edge mounted device;

(c) a method of increasing the proximity of active or passive devices on a circuit laminated substrate; embedding conductive leads in the laminated substrate parallel to the top and bottom surfaces; mounting an active or passive device on the top or bottom surface; providing a via extending from the top and/or the bottom planar surface into the substrate for the **attachment** of the mounted device to the conductive leads; **attaching** active or passive devices on the edge surface; and providing **connection** points on the edge surface for the **attachment** of an edge surface mounted active or passive devices through conductive leads and via to a top or bottom mounted device;and

(d) a device comprising a **multi-layered** circuit sub assembly, and a semiconductor chip (42).

USE - Used for rapidly passing optical data transmitted from a spectroscope through VCSEL and the electronic structure to a computer for diagnostics and analysis.

ADVANTAGE - The arrangement allows for very dense packaging of such devices on the sub assembly.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective of the sub assembly.

Substrate (10)
Edge surface (18a, 18b)
Semiconductor chip (42)
Contact pads (44)
Top surface (48)
pp; 10 DwgNo 1/6

62/3,AB/15 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014846086
WPI Acc No: 2002-666792/200271
XRAM Acc No: C02-187110
XRPX Acc No: N02-527674

Production of printed **circuit layer** for **printed circuit boards**, involves imagewise exposing and developing photoresist, and removing underlying portions of metal and conductive **layers**

Patent Assignee: OAK-MITSUI INC (OAKN)
Inventor: ANDRESAKIS J A
Number of Countries: 096 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200235897	A1	20020502	WO 2001US32400	A	20011017	200271	B
AU 200211790	A	20020506	AU 200211790	A	20011017	200271	
EP 1332653	A1	20030806	EP 2001979868	A	20011017	200353	
			WO 2001US32400	A	20011017		
KR 2003044046	A	20030602	KR 2003705804	A	20030425	200366	

Priority Applications (No Type Date): US 2000697614 A 20001026
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

WO 200235897 A1 E 26 H05K-003/06
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200211790 A H05K-003/06 Based on patent WO 200235897
EP 1332653 A1 E H05K-003/06 Based on patent WO 200235897
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
KR 2003044046 A H05K-003/06

Abstract (Basic): WO 200235897 A1
Abstract (Basic):

NOVELTY - A substrate is sequentially deposited with an electrically conductive **layer** surface (I), a thin metal **layer** on roughened surface (II) of electrically conductive **layer**, and a photoresist. The photoresist is imagewise exposed and developed, such that underlying portions of metal **layer** is removed thereby revealing underlying portions of conductive **layer**, which is then removed to produce a **printed circuit layer**.

DETAILED DESCRIPTION - An electrically conductive **layer** surface (I) is deposited on a substrate. The electrically conductive **layer** has a roughened surface (II) opposite to surface (I). Subsequently, a thin metal **layer** is deposited on the roughened surface (II) of the electrically conductive **layer**. The metal **layer** comprises a material having different etch resistance property than that of the electrically conductive **layer**. Subsequently, a photoresist is deposited on the metal **layer**. The photoresist is imagewise exposed and developed, thereby revealing underlying portions of the metal **layer**. The revealed underlying portions of the metal **layer** is removed thereby revealing underlying portions of the conductive **layer**. Subsequently, the revealed underlying portions of the conductive **layer** is removed to produce a **printed circuit layer**. INDEPENDENT CLAIMS are included for the following:

(1) Process for producing composite, which involves producing several **printed circuit layers**, and **attaching** the **printed circuit layers** to each other through at least one intermediate stratum, to form a **printed circuit board**; and

(2) **Printed circuit layer**.

USE - For producing **printed** circuit **layer** for **printed circuit boards**.

ADVANTAGE - The process for producing **printed circuit layer** eliminates the need for a black oxide treatment to improve adhesion, and improves the ability to optically inspect the **printed circuit boards**. Since the metal **layers** are highly uniform and reflective, the **printed circuit boards** are formed with compatibility with automatic optical inspection equipment. The metal **layers** have high mechanical strength, and are highly resistant to mechanical damage, such as surface scratches and scuff marks. The metal **layer** used in the production of **printed circuit layer** acts as an etch mask during conductive **layer** etching, and improves etch accuracy and resolution. After etching, the thin metal **layer** remains on the conductive **layer** obviating the need for an oxide **layer**.

pp; 26 DwgNo 0/0

62/3,AB/16 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014670047
WPI Acc No: 2002-490751/200252
XRAM Acc No: C02-139429
XRPX Acc No: N02-387932
Fiber-optical strain gauge includes mechanical construction comprising anchorage mechanisms, two **connecting** rods comprising articulated **connections** at both ends, and transmission construction **connected** to rod ends
Patent Assignee: VESTAS WIND SYSTEM AS (VEST-N); JENSEN J (JENS-I); JORGENSEN H S (JORG-I); KLEMAR B A (KLEM-I); VESTAS WIND SYSTEMS AS (VEST-N)
Inventor: JENSEN J; JORGENSEN H S; KLEMAR B A
Number of Countries: 095 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200252223	A1	20020704	WO 2000DK725	A	20001222	200252 B
EP 1346190	A1	20030924	EP 2000984928	A	20001222	200363
			WO 2000DK725	A	20001222	
US 20040035217	A1	20040226	WO 2000DK725	A	20001222	200416
			US 2003451239	A	20030620	

Priority Applications (No Type Date): WO 2000DK725 A 20001222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200252223	A1	E	15	G01B-011/16	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

EP 1346190	A1	E	G01B-011/16	Based on patent WO 200252223

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

US 20040035217	A1		G01L-001/24

Abstract (Basic): WO 200252223 A1
Abstract (Basic):
NOVELTY - A fiber-optical strain gauge includes a mechanical construction comprising anchorage mechanisms for providing two pointy-formed **connections** between the mechanical construction and an object to be measured on; two **connecting** rods comprising articulated **connections** at both ends; and a transmission construction **connected** to the rod ends opposite the respective anchorage mechanism.
DETAILED DESCRIPTION - A fiber-optical strain gauge comprises a mechanical construction, which provides a strain-dependent relative movement of oppositely positioned, spaced apart first and second optical fiber ends in a direction perpendicular to the axial direction of the optical fibers (7a, 7b). The mechanical construction uses the varying transmission of light between the two fibers as an indication of the strain. Fiber-holding elements (6a, 6b) are provided for **securing** the two fibers to the mechanical construction in an aligned relationship in the unstrained condition. The mechanical

construction comprises anchorage mechanisms (3a, 3b) for providing two pointy-formed **connections** between the mechanical construction and an object to be measured on. A line (8) through the two **connection** points defines as train-measuring direction. Two **connecting** rods (2a, 2b) are provided which extend in the strain-measuring direction. The rods comprise articulated **connections** to the respective anchorage mechanism at one end and to respective rods (5a-5d) forming a pantograph-like structure of the mechanical construction at the other end, respectively. A transmission construction is **connected** to the rod ends opposite the respective anchorage mechanism. The transmission construction is adapted for transferring the movement of the rods in the strain-measuring direction to the fiber-holding elements and for guiding the movement of the fiber-holding elements in a direction perpendicular to the axial direction of the optical fibers. An INDEPENDENT CLAIM is included for a method of mounting optical fibers in the inventive strain gauge. The method involves stripping protective **layers** from an optical fiber in the area of fixation, and mounting the stripped fiber in a **solder** and/or glue on the optical fiber-holding elements in a pre-stressed condition. After solidification of the **solder** and/or hardening of the glue, the fiber is scored and cleaved between the fixation points. A distance provided between the resulting fiber ends is dependent on the pre-stressing of the fiber during mounting.

USE - As a fiber-optical strain gauge.

ADVANTAGE - The arrangement of the inventive fiber-optical strain gauge makes it possible to provide strain gauge measurements, which are substantially not influenced by movements of the measuring points in directions in a plane perpendicular to the desired strain-measuring direction. With this arrangement, the movements of the measuring points are eliminated to a large extent by the **connecting** rods comprising articulated **connections** at both ends.

DESCRIPTION OF DRAWING(S) - The figure shows a portion of the fiber-optical strain gauge.

Connecting rods (2a, 2b)
Anchorage mechanisms (3a, 3b)
Fiber-holding elements (6a, 6b)
Optical fibers (7a, 7b)
Line (8)
pp; 15 DwgNo 3/7

62/3,AB/17 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014494473
WPI Acc No: 2002-315176/200235
XRAM Acc No: C02-091635
XRPX Acc No: N02-246735
Formulation for producing water-soluble and heat resistant deposit on substrate for producing **circuit board**, comprises preset amount of water soluble solid producing polymerizable ingredients, and carbohydrate
Patent Assignee: DYMAX CORP (DYMA-N)
Inventor: BACHMANN A G; CANTOR S E; LAM V V
Number of Countries: 087 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200204549	A1	20020117	WO 2001US40761	A	20010518	200235	B
AU 200163505	A	20020121	AU 200163505	A	20010518	200238	

Priority Applications (No Type Date): US 2000613884 A 20000711
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200204549 A1 E 17 C08J-005/10
Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200163505 A C08J-005/10 Based on patent WO 200204549

Abstract (Basic): WO 200204549 A1
Abstract (Basic):
NOVELTY - A formulation comprises (in weight parts) water soluble solid producing polymerizable ingredient(s) (20-60), carbohydrate (2-40) selected from group-I consisting of sorbitol, cyclodextrin compounds, fructose, xylose and/or starch, and water-soluble ingredient(s) (25-95) for controlling rheology and physical stability of the formulation.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for producing an article by applying the formulation to the surface of a substrate, curing to produce a solid deposit on the surface and washing the surface with water to remove the deposit.
USE - The method is used for producing highly water-soluble, water-washable, and heat resistant deposit upon substrate used to produce **printed circuit board**, for producing **solder** bearing articles, e.g. to serve as a water-soluble **adhesive** for temporary tacking, bonding or mounting of a component, to serve as a removable marking system and as a readily removable protective barrier **layer**, to provide temporary **spacers**, etc.
ADVANTAGE - The free radical generating catalyst initiates polymerization of the polymerizable ingredients, and stabilizer prevents premature polymerization of the polymerization ingredients. The formulation satisfies criteria for **solder** resist, or for a similar material that is used in producing a high temperature, water-soluble **coating** or other deposit. The deposit resists high temperatures and functions as an effective **solder** resist maskant. The cured deposit can be readily, thoroughly, and rapidly removed, using relatively mild washing conditions, to produce a water stream that does not unduly contaminate, clog, or otherwise disable downstream water-treatment materials or units. The formulation is homogeneous and stable against separation, and is readily applied to the substrate. The formulation provides fast and complete cure, good adhesion to the underlying surface in the cured state, and excellent resistance to deterioration and displacement. The gradually heating of deposit-bearing substrate, prior to immersion in the hot **solder**, tempers the deposit and reduces cracking and delamination.
pp; 17 DwgNo 0/0

62/3,AB/18 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014293372
WPI Acc No: 2002-114074/200215
XRAM Acc No: C02-034894

XRPX Acc No: N02-085116
Positioning of **multiple layers** that are stacked to form **multi-layer printed circuit** comprises determining characteristic values of electromotive forces and/or currents electromagnetically induced in other fixed multiple circuits
Patent Assignee: BALLADO INVESTMENTS INC (BALL-N)
Inventor: AMMANN B
Number of Countries: 095 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200180613	A1	20011025	WO 2001IB152	A	20010207	200215	B
AU 200128747	A	20011030	AU 200128747	A	20010207	200219	
US 6367678	B1	20020409	US 2000551884	A	20000418	200227	
EP 1275277	A1	20030115	EP 2001969066	A	20010207	200306	
			WO 2001IB152	A	20010207		
JP 2003531482	W	20031021	JP 2001576730	A	20010207	200373	
			WO 2001IB152	A	20010207		

Priority Applications (No Type Date): US 2000551884 A 20000418
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200180613	A1	E	17	H05K-003/46	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200128747	A		H05K-003/46	Based on patent WO 200180613
US 6367678	B1		B23K-031/12	
EP 1275277	A1	E	H05K-003/46	Based on patent WO 200180613

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

JP 2003531482	W	16	H05K-003/46	Based on patent WO 200180613

Abstract (Basic): WO 200180613 A1
Abstract (Basic):
NOVELTY - Positioning of **multiple layers** that are stacked to form a **multi-layer printed circuit** involves determining the characteristic values electromotive forces and/or currents which in turn are electromagnetically induced by the current in other fixed multiple circuits. The multiple circuits are arranged parallel to closed circuit(s).
DETAILED DESCRIPTION - Positioning of **multiple layers** that are stacked to form a **multi-layer printed circuit** involves producing flat continuous closed circuit (3) on the outermost parts of the peripheral edges of each **layer**. Multiple fixed circuits (4, 4e) that are applied to a reference board (7) are arranged parallel to the closed circuit so that each circuit has a portion superimposed on the closed circuit. An alternating current of desired frequency is injected into one of the multiple circuits which results in the generation by electromagnetic induction of an induced current that flows in the closed circuit(s). The characteristic values of electromotive forces (En) and/or currents are determined which are in turn electromagnetically induced by the current in other fixed multiple circuits arranged parallel to the closed circuit. Rotational-translational displacement of the **layer** is executed on at least one closed circuit relative to the multiple fixed circuits. The closed circuit ensures that the characteristic values of electromotive forces (En) and/or currents (In) relative to the current assume values that indicate part of each **multiple layer** is

stacked in a predetermined position relative to a portion of the closed circuit. The **layer** is picked-up and transferred without altering its angular orientation w.r.t the vertical and horizontal planes to a position where it is to be inserted in order to form a **multi-layer printed circuit**. It is **attached** to the parallel stacked **layers** of the **printed circuit**. The **multi-layer printed circuit** is removed after all **layers** have been interconnected.

USE - For positioning **multiple layers** that are stacked to form a **multi-layer printed circuit**.

ADVANTAGE - The process provides accurate positioning of various stacked **layers** which has margins of error times smaller than those that apply to circuits assembled by the conventional process. It reduces the order of magnitude of the **multi-layer** circuit drilling and stacking error, thus avoiding the need to take x-ray measurements. The determination of the characteristic values of the electromotive forces and/or currents provides correct positioning of the **layer** on which the circuit is **attached**.

DESCRIPTION OF DRAWING(S) - The figure shows a basic diagram of the process.

Closed circuit (3)
Fixed circuits (4, 4e)
Reference board (7)
pp; 17 DwgNo 1/4

62/3,AB/19 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014196649
WPI Acc No: 2002-017346/200202
Related WPI Acc No: 1999-551017; 1999-551018; 1999-551019; 1999-551020; 1999-551021; 1999-551022; 2000-350122; 2000-364682; 2001-244130; 2001-257406; 2001-257524; 2001-389548; 2002-034088; 2002-034089; 2002-041186; 2002-041187; 2002-041188; 2002-049008; 2002-049009; 2002-689464; 2002-730929; 2003-015741; 2004-118800
XRAM Acc No: C02-004890
XRPX Acc No: N02-013912
Fabric for use in electronic packaging applications, comprises fiber strand(s) of several fibers **coated** with **resin** compatible composition, which has preset air jet compatibility
Patent Assignee: PPG IND OHIO INC (PITT)
Inventor: LAMMON-HILINSKI K; LAWTON E L; NOVICH B E; RICE W B; ROBERTSON W J; VELPARI V; WU X
Number of Countries: 096 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200168752	A1	20010920	WO 2001US8684	A	20010316	200202	B
AU 200145851	A	20010924	AU 200145851	A	20010316	200208	
BR 200109277	A	20021210	BR 20019277	A	20010316	200308	
			WO 2001US8684	A	20010316		
EP 1272550	A1	20030108	EP 2001918815	A	20010316	200311	
			WO 2001US8684	A	20010316		
KR 2002086924	A	20021120	KR 2002712204	A	20020916	200320	
US 6593255	B1	20030715	US 9834056	A	19980303	200348	
			US 9834077	A	19980303		
			US 9834078	A	19980303		
			US 9834525	A	19980303		
			US 9834663	A	19980303		

				US 98130270	A	19980806	
				US 98170566	A	19981013	
				US 98170578	A	19981013	
				WO 99US21443	A	19991008	
				US 2000527034	A	20000316	
				US 2000548379	A	20000412	
				US 2000568916	A	20000511	
				US 2000620523	A	20000720	
				US 2000620524	A	20000720	
				US 2000620525	A	20000720	
				US 2000620526	A	20000720	
				US 2000705353	A	20001103	
JP 2003526593	W	20030909	JP 2001567240	A	20010316	200360	
			WO 2001US8684	A	20010316		
CN 1437628	A	20030820	CN 2001809658	A	20010316	200374	
TW 544444	A	20030801	TW 2001106185	A	20010316	200411	

Priority Applications (No Type Date): US 2000705353 A 20001103; US 2000527034 A 20000316; US 2000548379 A 20000412; US 2000568916 A 20000511 ; US 2000620523 A 20000720; US 2000620524 A 20000720; US 2000620525 A 20000720; US 2000620526 A 20000720; US 9834056 A 19980303; US 9834077 A 19980303; US 9834078 A 19980303; US 9834525 A 19980303; US 9834663 A 19980303; US 98130270 A 19980806; US 98170566 A 19981013; US 98170578 A 19981013; WO 99US21443 A 19991008

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200168752	A1	E	161	C08J-005/08	
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW				
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW					
AU 200145851	A			C08J-005/08	Based on patent WO 200168752
BR 200109277	A			C08J-005/08	Based on patent WO 200168752
EP 1272550	A1	E		C08J-005/08	Based on patent WO 200168752
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
KR 2002086924	A			C03C-025/10	
US 6593255	B1			B32B-009/00	CIP of application US 9834056 CIP of application US 9834077 CIP of application US 9834078 CIP of application US 9834525 CIP of application US 9834663 CIP of application US 98130270 CIP of application US 98170566 CIP of application US 98170578 CIP of application WO 99US21443 Cont of application US 2000527034 Cont of application US 2000548379 Cont of application US 2000568916 Cont of application US 2000620523 Cont of application US 2000620524 Cont of application US 2000620525 Cont of application US 2000620526 Cont of patent US 6419981
JP 2003526593	W		197	C03C-025/10	Based on patent WO 200168752
CN 1437628	A			C08J-005/08	
TW 544444	A			C03C-025/10	

Abstract (Basic): WO 200168752 A1

Abstract (Basic):

NOVELTY - A fabric comprises fiber strand(s) (10) comprising several fibers (12) provided with a **resin** compatible **coating** (14) on the surface (16). The strand has an Air Jet Transport Drag Force Value of 100000 gram force/gram mass or more, determined by a needle air jet nozzle unit having an internal air jet chamber of 2 mm diameter and a nozzle exit tube of length 20 cm at a strand feed rate of 274 m/minute and an air pressure of 310 kiloPascals.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a reinforced laminate comprising a matrix material and the fabric.

USE - For reinforced laminates (claimed) used in electronic packaging applications and as reinforcement for telecommunication cables.

ADVANTAGE - The composites or laminates formed from fiber strands woven into fabrics provides good wet-through and good wet-out properties of strands. The **coating** on the surfaces of fiber strands protect the fiber from abrasion and breakages during processing and provide good weavability particularly on air jet looms and increased productivity. The fiber strand is compatible with **polymeric** matrix **material**. The **coated fiber glass** strands have low fuzz and halos, low broken filaments, low strand tension, high pliability and low insertion time and facilitates weaving and knitting to provide fabric with few surface defects. The **coated** fiber strands facilitates thermal conduction along **coated** surfaces of fiber. When used as continuous reinforcement for electronic **circuit boards**, the **coated** glass fibers promotes heat dissipation from a heat source (such as chip or circuit) along the reinforcement to conduct heat away from electronic components and thereby inhibiting thermal degradation and/or deterioration of circuit components, glass fibers and **polymeric** matrix **material**. The **coated** glass fibers provide higher thermal conductivity phase than matrix material, thereby reducing differential thermal expansion and warpage of electronic **circuit board** and improving **solder** joint reliability. Need for incorporating thermally conductive material in the matrix **resin** is avoided, hence laminate manufacturing operations are improved at low cost. The strands posses high strand openness (enlarged cross sectional area and the filaments of strand are not tightly bound to one another) which can facilitate penetration or wet-out of matrix material into the strand bundles. The laminates made from fiber strands has low coefficient of thermal expansion, good flexural strength, good interlaminar bond strength and good hydrolytic stability. Electronic supports and **printed circuit boards** formed from the fiber strands has good drillability and resistance to metal migration. Production cycle time is reduced, capital equipment is eliminated, fabric handling and labor cost are reduced and fabric quality and product properties are improved. Abrasive wear of fiber strands are inhibited when contacted with solid objects such as portions of winding, weaving or knitting device or by interfilament abrasion. The **coating** composition are substantially free of heat expandable particles. Good **resin** penetration is enabled into warp yarn bundles during lamination and improves overall hydrolytic stability of laminates and electronic supports by reducing or eliminating paths of ingress for moisture into the laminates and electronic supports. Electrical short failures due to formation of conductive anodic filaments when exposed under bias to humid condition, is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a **coated** fiber strand.

Fiber strand (10)
Fibers (12)
Coating (14)
Surface (16)
Particles (18)
pp; 161 DwgNo 1/13

62/3,AB/20 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013788551
WPI Acc No: 2001-272762/200128
Related WPI Acc No: 2000-115265; 2002-163618
XRAM Acc No: C01-082682
XRPX Acc No: N01-194755
Microelectronic component for mounting hybrid **circuit** to **printed circuit board**, includes flexible interposer which overlies rigid interposer
Patent Assignee: TESSERA INC (TESS-N)
Inventor: BELLAAR P H; DISTEFANO T H; FJELSTAD J; PICKETT C M; SMITH J W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6208025	B1	20010327	US 97978082	A	19971125	200128 B
			US 99413410	A	19991006	

Priority Applications (No Type Date): US 97978082 A 19971125; US 99413410 A 19991006
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6208025	B1		9	H01L-023/48	Div ex application US 97978082

Abstract (Basic): US 6208025 B1
Abstract (Basic):
NOVELTY - A microelectronic component comprises a first interposer having contacts for mounting and electrically **connecting** a semiconductor chip. A second interposer is overlying the first interposer. It comprises a top and a bottom surface, and is more flexible than the first interposer.
DETAILED DESCRIPTION - A microelectronic component comprises a first interposer (110) having contacts (113). The first interposer is adapted for mounting and electrically **connecting** a semiconductor chip. A second interposer (114) overlies the first interposer. It comprises a top (115) and a bottom surface (116), and is more flexible than the first interposer. Terminals (118) are exposed to the bottom surface of the second interposer. Electrical **connections** (119) **connect** the terminals to the contacts. The terminals are movable relative to the contacts to compensate for thermal expansion of the first interposer. An INDEPENDENT CLAIM is also included for a socket assembly for the microelectronic component comprising a sheet-like dielectric socket body (101) having a first (102) and a second surface (103), and apertures (104). Resilient socket contacts (105) extend into associated apertures, and socket terminals (106) are electrically **connected** to the socket contacts.
USE - The microelectronic component is used for mounting and/or testing semiconductor chips and related electronic components. It is particularly useful for mounting a hybrid **circuit** to a printed **circuit board**.

ADVANTAGE - The inventive microelectronic component eliminates warpage or distortion of the semiconductor chips or substrate during interconnection. The flexible interposer facilitates movement of the contact ends of the leads relative to the terminals, thus contributing to the ability of the chip carrier to withstand thermal cycling.

DESCRIPTION OF DRAWING(S) - The figure shows a diagrammatic sectional view of a semiconductor chip assembly.

Sheet-like dielectric socket body (101)
First surface (102)
Second surface (103)
Apertures (104, 117)
Resilient socket contacts (105)
Socket terminals (106)
Solid spherical core (108)
First interposer (110)
Contacts (113)
Second interposer (114)
Top surface (115)
Bottom surface (116)
Terminals (118)
Electrical **connections** (119)
Joining units (120)
Solid core (121)
Solder coated copper ball (122)
Electrically conductive **spacers** (123)
Compliant **layer** (124)
pp; 9 DwgNo 3/3

62/3,AB/21 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013169770
WPI Acc No: 2000-341643/200030
Related WPI Acc No: 1995-163252; 2000-341642; 2000-389286
XRAM Acc No: C00-103819
XRPX Acc No: N00-256668
Electronic packaging interconnect structure for comprises two rigid, confronting substrates joined by **solder ball connected** to joining materials on contacts of respective substrates
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ACOCELLA J; BANKS D R; BENENATI J A; CAULFIELD T; CORBIN J S; HOEBENER K G; WATSON D P
Number of Countries: 011 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1002611	A1	20000524	EP 94114605	A	19940916	200030	B
			EP 99125770	A	19940916		

Priority Applications (No Type Date): US 93144981 A 19931028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1002611	A1	E	27	B23K-001/00	Div ex application EP 94114605 Div ex patent EP 650795

Designated States (Regional): AT BE CH DE ES FR GB IT LI NL SE

Abstract (Basic): EP 1002611 A1
Abstract (Basic):
NOVELTY - Interconnect structure includes first joining material

for each pair of contacts **connected** to respective contact of first interconnect substrate and second joining material for each pair of contacts **connected** to respective contact of second interconnect substrate. Melting temperatures of joining materials are lower than that of conductive metal balls for respective metal contact pairs.

DETAILED DESCRIPTION - An interconnect structure comprises:

(a) first and second interconnect substrates;

(b) a planar pattern of multiple, metal contacts on each of the substrates;

(c) a ball of conductive metal for respective pairs of such contacts with a diameter about the same as the width of the contacts; and

(d) a volume of first joining material for each such pair of contacts **connected** to the respective contact of the first interconnect substrate and a volume of the second joining material for each such pair of contacts **connected** to the respective contact of the second interconnect substrate, with melting temperatures of the joining materials of both the first and second volumes substantially less than the melting temperature of the metal balls, with the first and second volumes of each pair of contacts **connected** to approximately diametrically opposite ends of a respective metal ball, and with the smallest cross-sectional area of each joining material volume having a minimum diameter of at least about two-thirds of the diameter of the metal ball.

The diameter of the metal balls and the widths of the contacts are 0.6-1.2 mm, and the minimum of such cross-section of each joining material volume is at least about 0.6 mm.

Preferably, the contacts are round with a diameter of 0.7 mm, and the diameter of the metal balls is about 0.9 mm.

An INDEPENDENT CLAIM is given for an interconnect structure.

USE - **Connection** of two rigid, confronting substrates using high melting temperature **solder ball connections** to form an electronic packaging structure.

ADVANTAGE - A more symmetrical and reliable **solder** joint is formed.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of an embodiment of the invention illustrating a **multilayer** ceramic chip carrier with **solder balls attached** to contacts and confronting mirror image contacts of a **fiberglass**-epoxy **circuit board**.

Ceramic chip carrier substrate (10)

Second substrate, especially **fiberglass**-epoxy **circuit board** (11)

Contacts (12)

Joining material (13, 16)

Vias (14, 15)

Contacts (17)

Solder balls (18)

pp; 27 DwgNo 4/19

62/3,AB/22 (Item 17 from file: 350)

013169769
WPI Acc No: 2000-341642/200030
Related WPI Acc No: 1995-163252; 2000-341643; 2000-389286
XRAM Acc No: C00-103818

XRPX Acc No: N00-256667
Connecting two rigid, confronting substrates involves using high melting temperature lead-tin **solder balls connected** to ceramic chip carrier substrate pads and eutectic lead-tin **solder balls** on **fiberglass**-epoxy **circuit board** pads

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ACOCELLA J; BANKS D R; BENENATI J A; CAULFIELD T; CORBIN J S; HOEBENER K G; WATSON D P

Number of Countries: 011 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1002610	A1	20000524	EP 94114605	A	19940916	200030 B
			EP 99125769	A	19940916	

Priority Applications (No Type Date): US 93144981 A 19931028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1002610	A1	E	28	B23K-001/00	Div ex application EP 94114605 Div ex patent EP 650795

Designated States (Regional): AT BE CH DE ES FR GB IT LI NL SE

Abstract (Basic): EP 1002610 A1
Abstract (Basic):

NOVELTY - High melting temperature Pb/Sn 95/5 **solder balls** are **connected** to Cu pads on ceramic chip carrier substrate (10) bottom by low melting temperature eutectic Pb/Sn **solder** by quick **reflow** to prevent Pb dissolution into eutectic **solder** and raising its melting temperature. Module is placed on **fiberglass**-epoxy **circuit board** with **solder balls** on eutectic Pb/Sn **solder bumps** on Cu pads of board.

DETAILED DESCRIPTION - Production of an interconnect assembly comprises:

(a) producing a first substrate with an approximately planar pattern of multiple, metal contacts on a major surface;

(b) depositing a volume of a first joining material on each of the contacts of the first substrate;

(c) **connecting** a conductive metal column to the first joining material on each of the contacts of the first substrate for maintaining a predetermined distance between the first substrate and a second substrate when **connected**;

(d) producing a second substrate with a major surface having an approximately planar pattern of multiple, metal contacts which are approximately a mirror image of the pattern of contacts of the first substrate;

(e) depositing a volume of a second joining material for positioning between the metal columns and each respective contact of the second substrate;

(f) positioning the substrates together for interconnection with contact patterns parallel, with mirror image pairs of contacts in confronting approximate alignment, and with each volume of the second joining material approximately in contact with a respective end of the metal column and a respective contact of the second substrate;

(g) simultaneously melting the first and second joining materials while the substrates ate positioned together, at a temperature at which the metal columns remain solid for providing the predetermined separation between substrates, for moving the ends of the metal columns by surface tension of the melted joining material to positions approximately at the center of the contacts; and

(h) cooling the substrates below the melting temperature of the

joining materials to form electrical interconnections between pairs of contacts.

INDEPENDENT CLAIMS are given for:
(A) an interconnect apparatus;
(B) a fabricated interconnect apparatus; and
(C) a second process for producing an interconnect structure.

USE - **Connection** of two rigid, confronting substrates using high melting temperature **solder ball connections** to form an electronic packaging structure.

ADVANTAGE - A more symmetrical and reliable **solder** joint is formed.

DESCRIPTION OF DRAWING(S) - First substrate (10)
Contacts (12)
First joining material (16)
Solder balls (18)
Sticky flux **layer** (20)
pp; 28 DwgNo 5/19

62/3,AB/23 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012989338
WPI Acc No: 2000-161191/200014
XRAM Acc No: C00-050490
XRPX Acc No: N00-120215
Thermistor device for use in assembling **circuit boards** comprises a thermistor element having conductive coatings which are electrically **connected** to external contacts on an electrically insulating substrate
Patent Assignee: SENSOR SCI INC (SENS-N)
Inventor: BRINLEY R G; GLINIECKI R M; HOWARD W N; BRINLEY G R
Number of Countries: 086 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200004560	A1	20000127	WO 99US16074	A	19990716	200014	B
AU 9951051	A	20000207	AU 9951051	A	19990716	200029	
GB 2357899	A	20010704	WO 99US16074	A	19990716	200138	
			GB 20011916	A	20010124		

Priority Applications (No Type Date): US 9897435 P 19980821; US 9893200 P 19980717
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200004560	A1	E	24	H01C-007/10	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9951051	A	H01C-007/10	Based on patent WO 200004560
GB 2357899	A	H01C-001/034	Based on patent WO 200004560

Abstract (Basic): WO 200004560 A1
Abstract (Basic):
NOVELTY - A surface mounted thermistor device comprises a thermistor element having top and bottom faces (20, 30), and a carrier substrate made of an electrically insulating material. The faces have

top and bottom conductive coatings (25, 35) and the substrate has a bottom face with first and second external contacts. The two contacts are in electrically communication with the conductive coatings.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of making a surface mounted thermistor device (10). The method includes: (a) forming a patterned conductive **coating** on an insulating carrier substrate (40); (b) providing electrical continuity between electrical contacts; (c) mounting a thermistor element on an internal contact; (d) providing internal electrical continuity between the thermistor element and the substrate; (e) optionally trimming the resistance values of the device; and (f) forming an encapsulation over the active thermistor element (15).

USE - The thermistor device is used in assembling **circuit boards**.

ADVANTAGE - Improved and economical thermistor device is obtained. The device has a uniform package size and excellent tolerance. The surface mount thermistor can be provided in resistance values and with resistance temperature response characteristics matching those of conventional wafer-style thermistor products.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of a thermistor device.

Thermistor device (10)
Thermistor element (15)
Top face (20)
Top conductive **coating** (25)
Bottom face (30)
Bottom conductive **coating** (35)
Carrier substrate (40)
First external contact (50)
Second external contact (55)
Conductive **connector** (60)
First internal contact (70)
Second internal contact (75)
Intermediate segments (80, 90)
Conductive band (85)
pp; 24 DwgNo 1/7

62/3,AB/24 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04292126
PRINTED-CIRCUIT BOARD

PUB. NO.: 05-283826 [JP 5283826 A]
PUBLISHED: October 29, 1993 (19931029)
INVENTOR(s): TSUJIOKA NORIO
TSUTSUI SHINICHI
APPLICANT(s): ASAHI SHIYUEEBELL KK [463978] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-401218 [JP 90401218]
FILED: December 11, 1990 (19901211)
JOURNAL: Section: E, Section No. 1501, Vol. 18, No. 66, Pg. 146, February 03, 1994 (19940203)

ABSTRACT

PURPOSE: To provide a **printed-circuit board** with good drillability, strong resis tance to **soldering** heat, good insulation property, and strong resistance to corro sion, by using reinforcement

composed of woven organic material that is **coated** with porous gel.

CONSTITUTION: A **printed-circuit board** is reinforced by woven organic material that is **coated** with porous gel obtained by condensation of one or more metal alkoxide compounds. Preferably, the metal alkoxide is silicon alkoxide, titanium alkoxide, aluminum alkoxide, or zirconium alkoxide. To manufacture the board, the metal alkoxide is dissolved in water or aqueous alcohol. The solution, containing a metal oxide precursor **polymer**, is spread on woven **fiberglass** sheets and heated, and then they are **coated** with metal oxide gel. The woven sheets are impregnated with **resin** to form prepregs, and they are laminated and heated under pressure to obtain an integral board.